

Model Name:GA-MA785GM-US2H

Component value change history

Version: 1.3

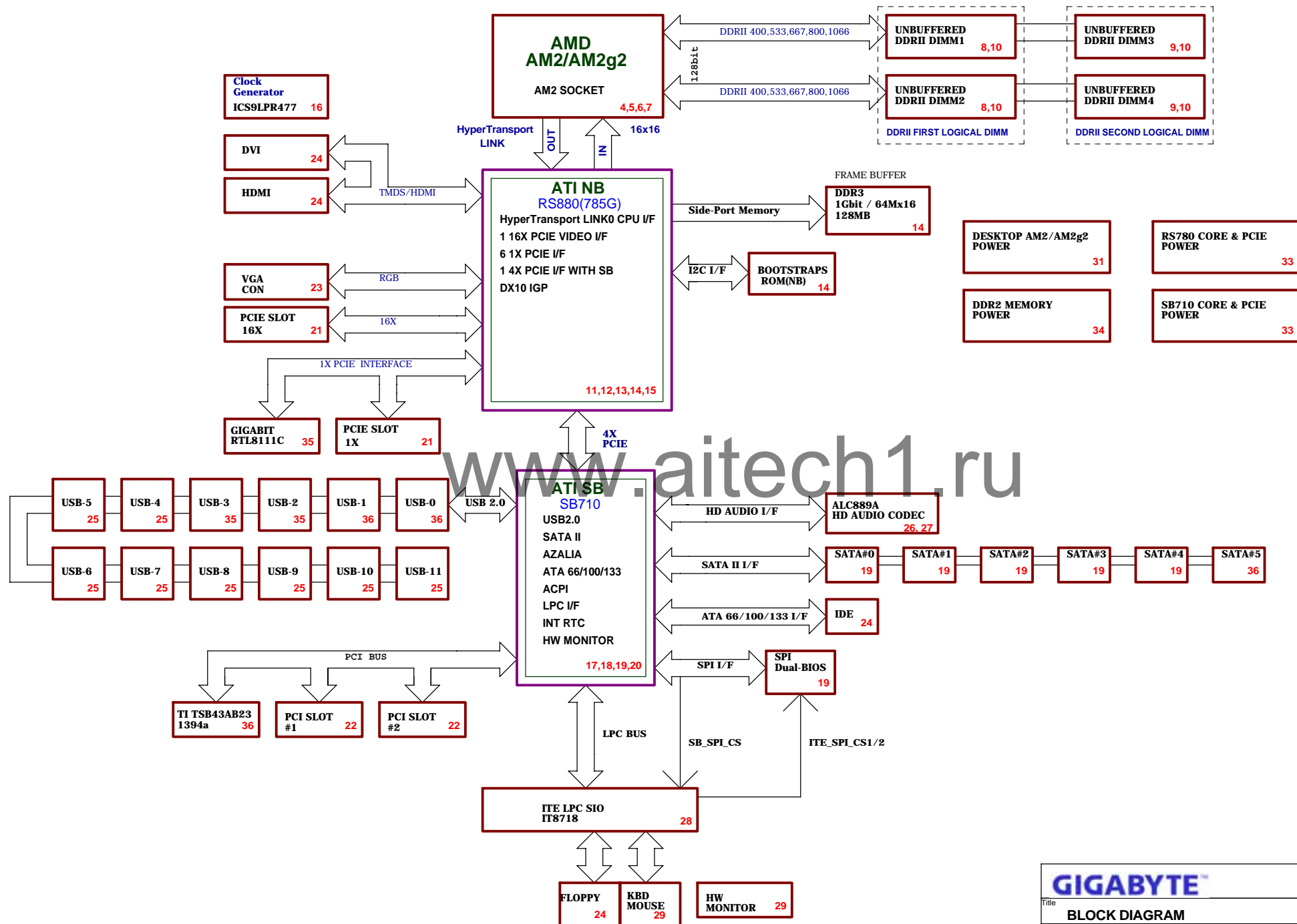
P-Code: U97028-0

[illegible]

Circuit or PCB layout change for next version

[illegible]

RS880 CUSTOMER DESKTOP REFERENCE DESIGN



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L0_CADIN_H[0..15] < L0_CADIN_H[0..15] 11

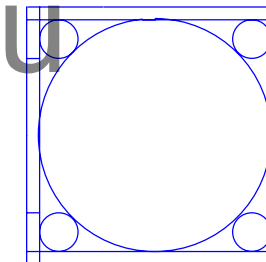
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L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] 11



CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPU
AM3RM/SC/BL/MB[12KRC-04K812-11R]

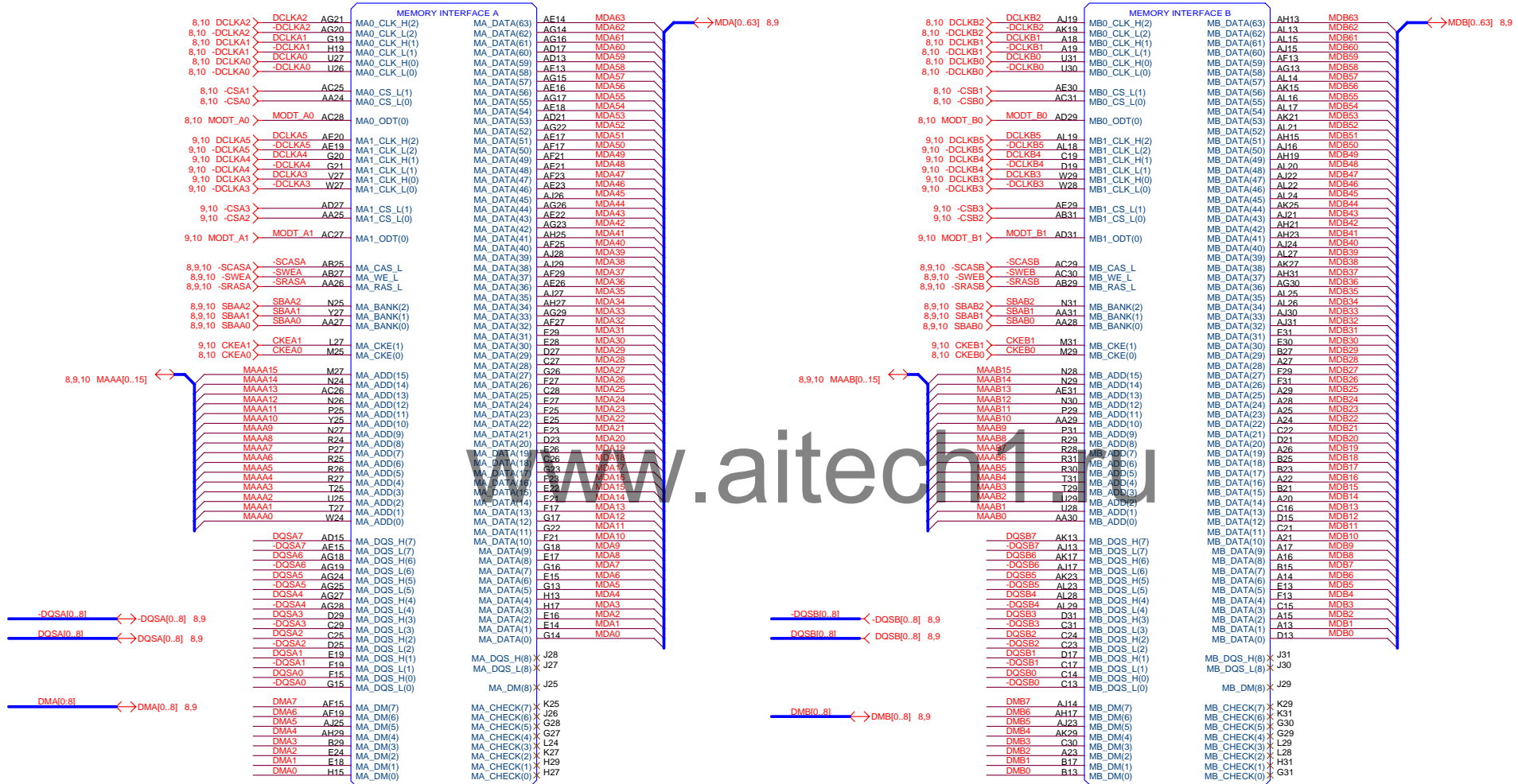


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Title			CPU HYPER TRANSPORT		
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M2CPUB

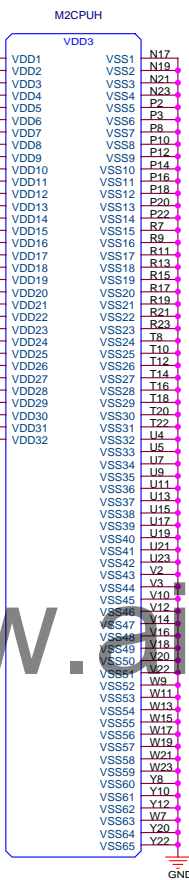
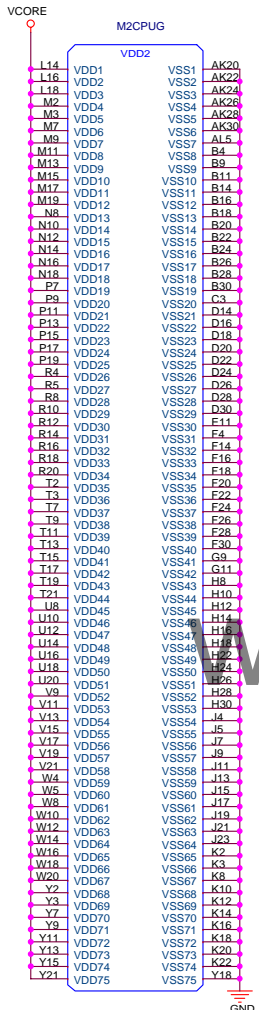
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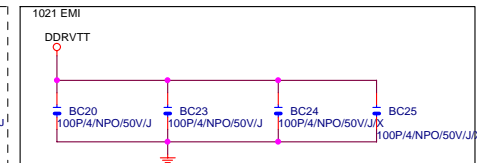
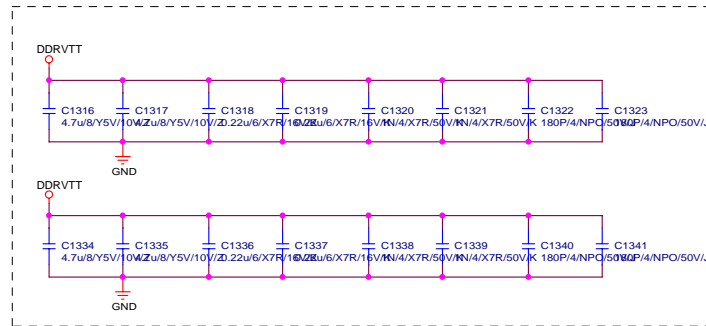
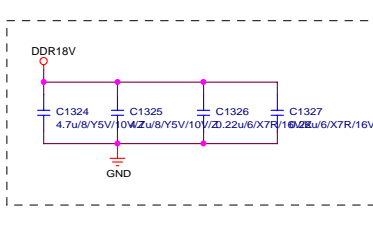
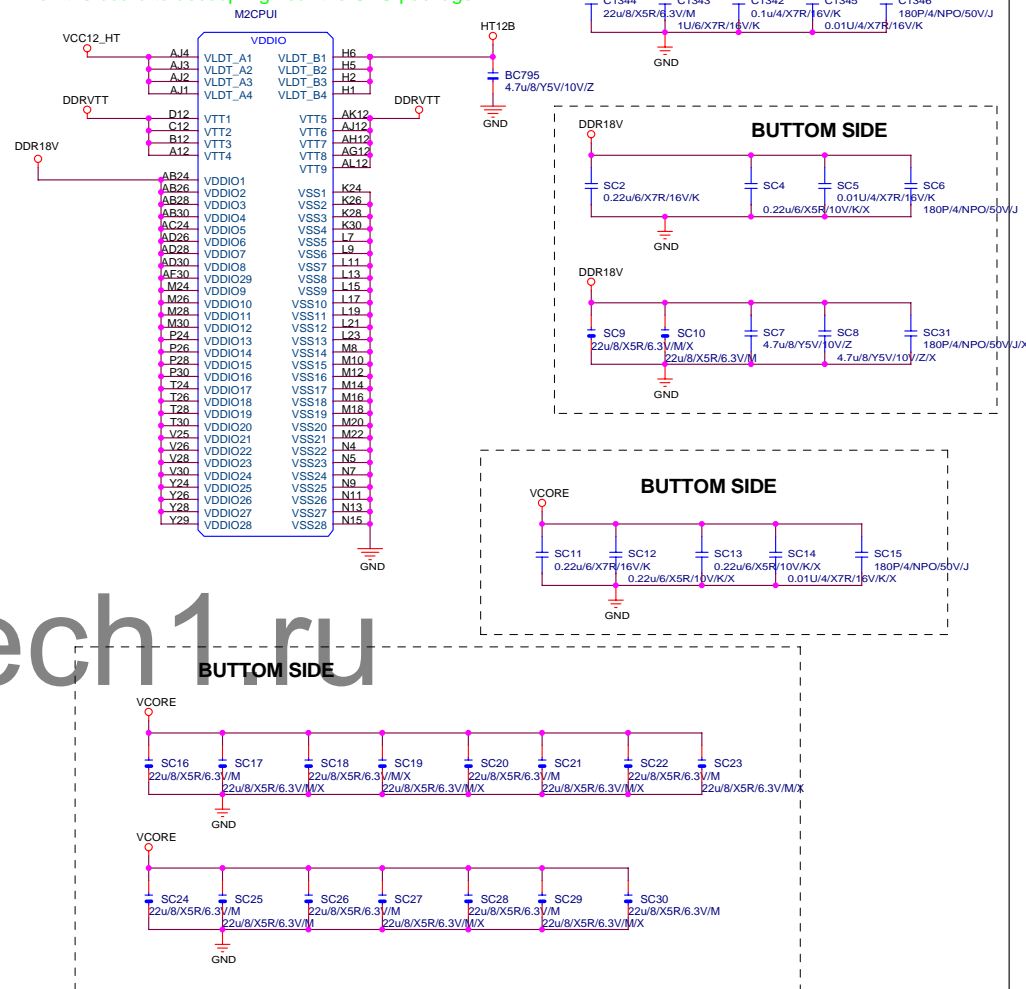
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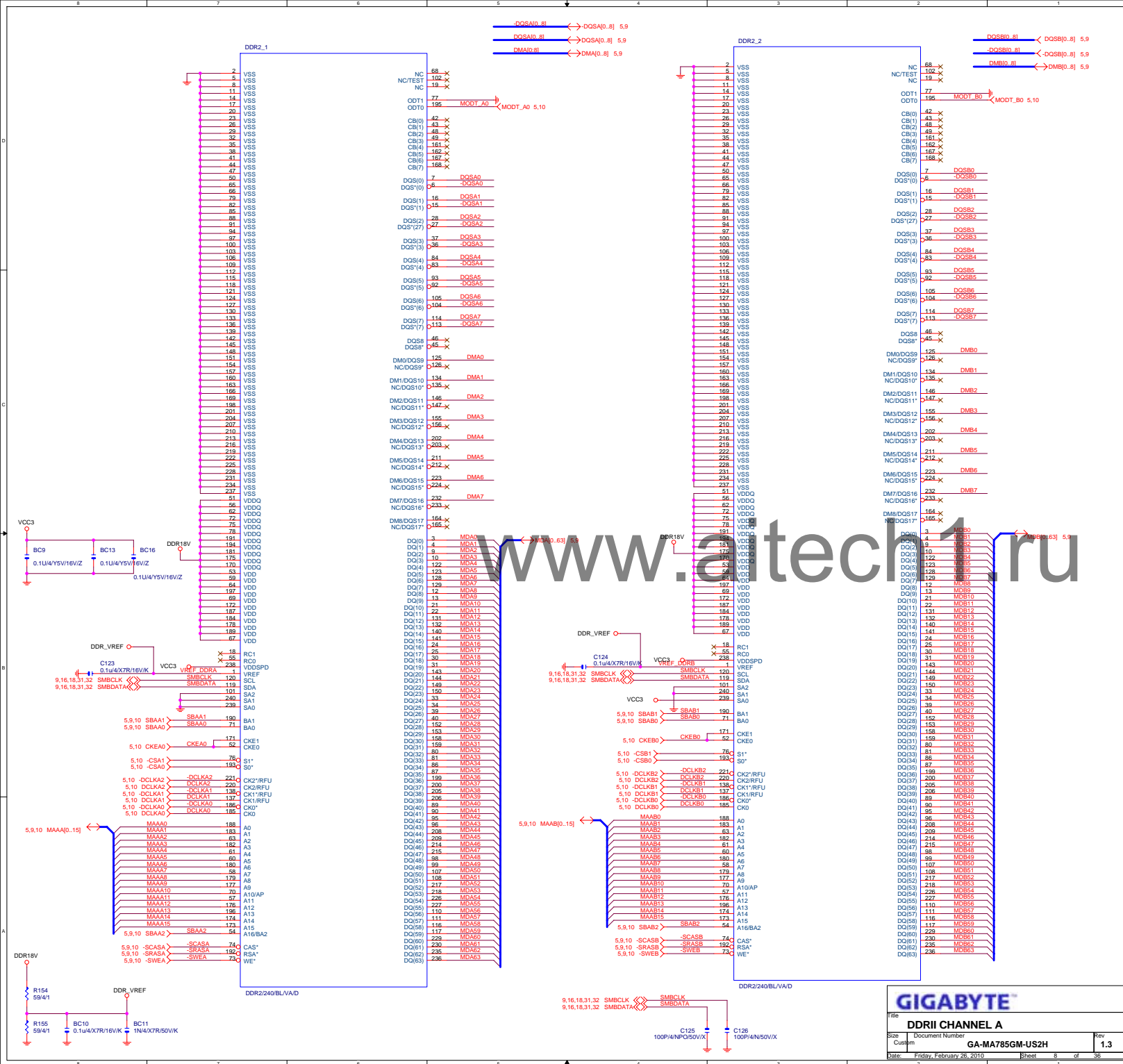
CPU DDRII MEMORY

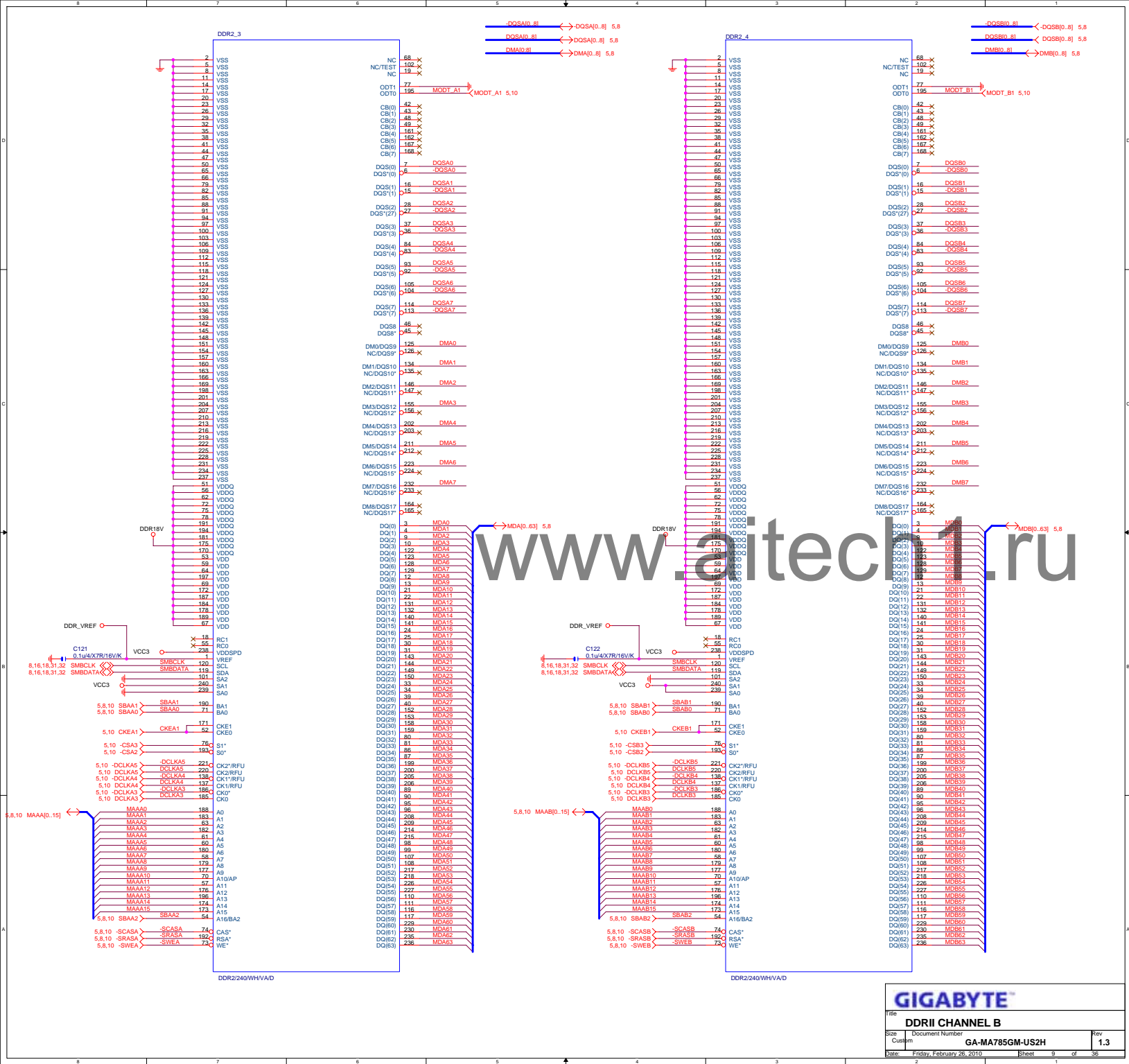
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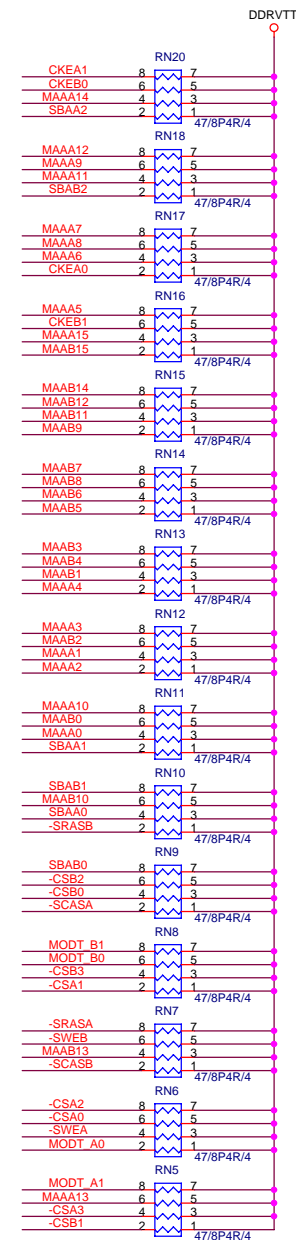
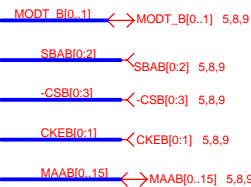
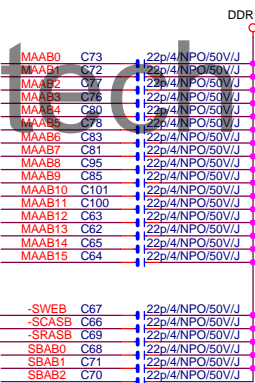
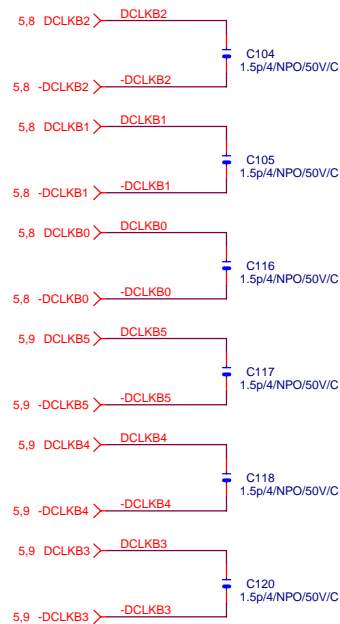
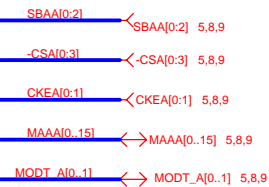
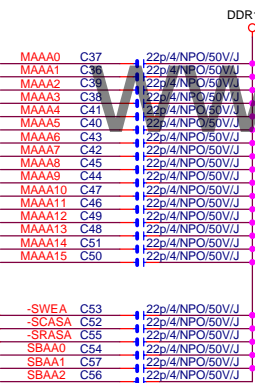
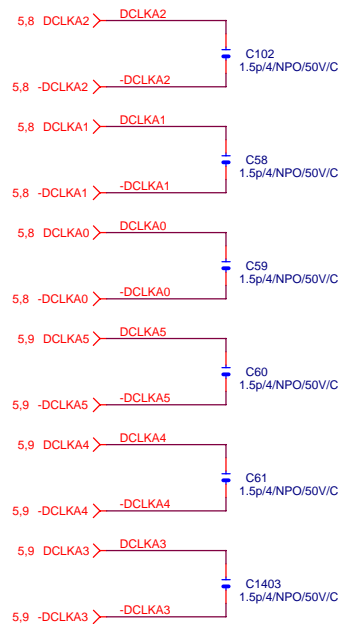
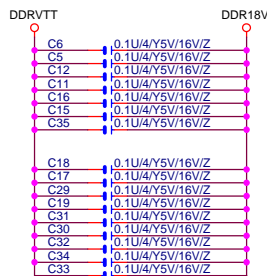
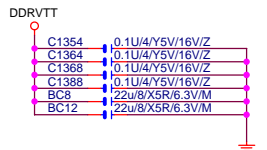


VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.









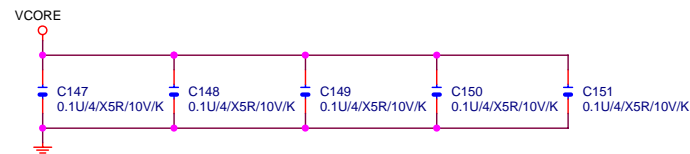
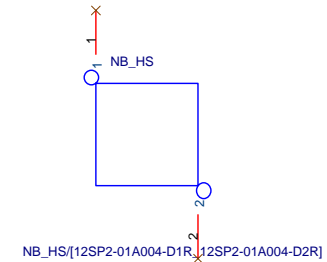


L0 CADIN L[0..15] L0_CADIN_L[0..15] 4

L0 CADIN H[0..15] L0_CADIN_H[0..15] 4

L0 CADOUT L[0..15] L0_CADOUT_L[0..15] 4

L0 CADOUT H[0..15] L0_CADOUT_H[0..15] 4

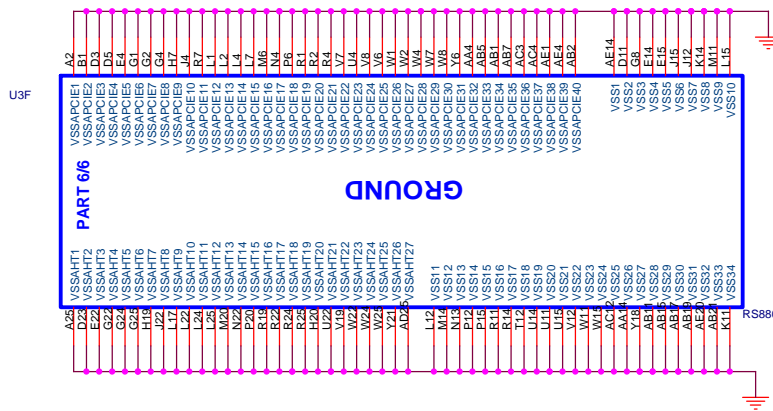


HT Link Stitching Caps

GIGABYTE™		
Title RS880 HT-LINK I/F		
Size B	Document Number GA-MA785GM-US2H	Rev 1.3
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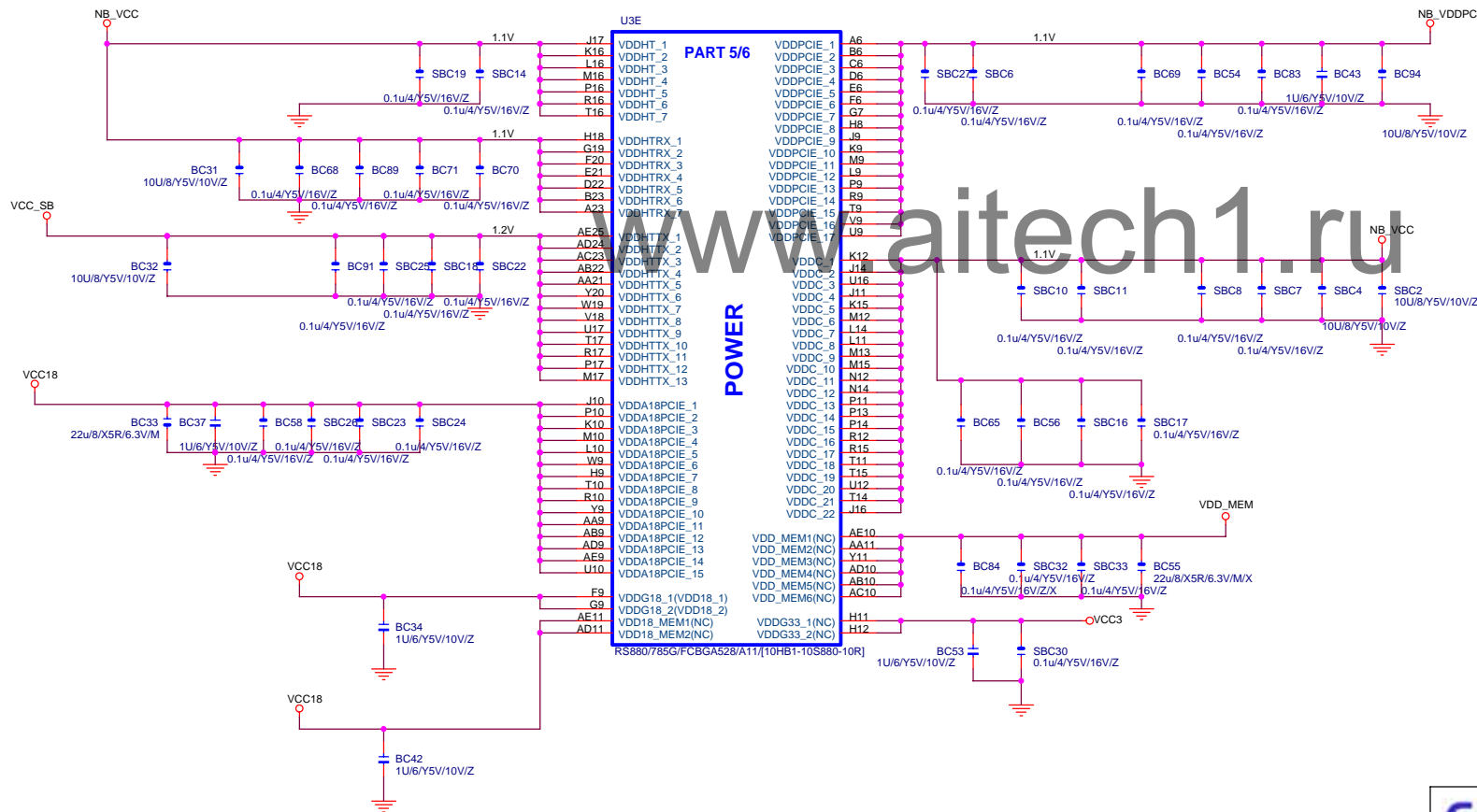






RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC



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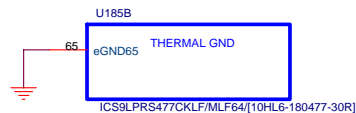


- Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK



NB CLOCKS		RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF		
HT_REFCLKN	NC	100M DIFF	100M DIFF		
REFCLK_P					
REFCLK_N	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF	
	NC	NC	vref	100M DIFF	
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF		
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)		
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF		

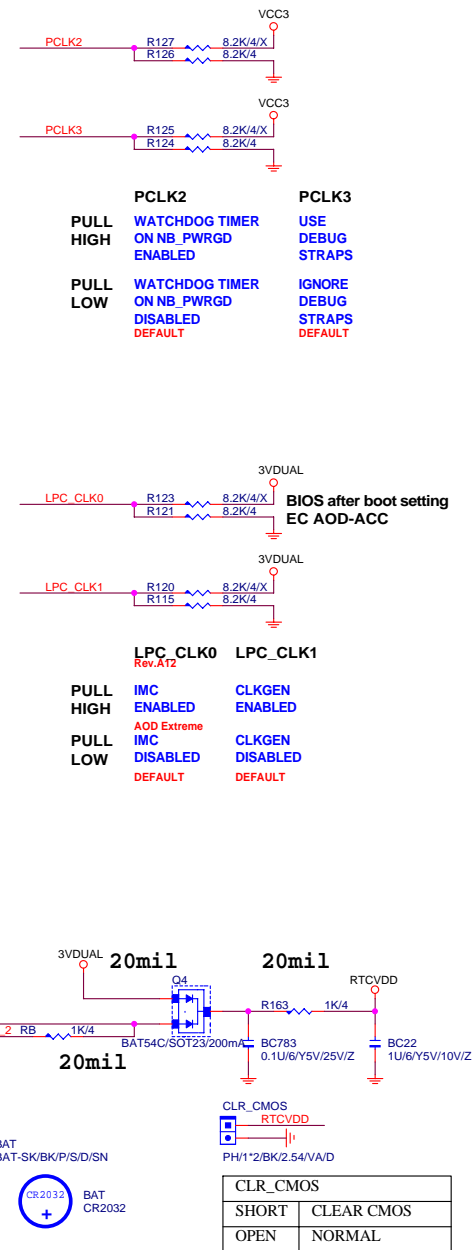
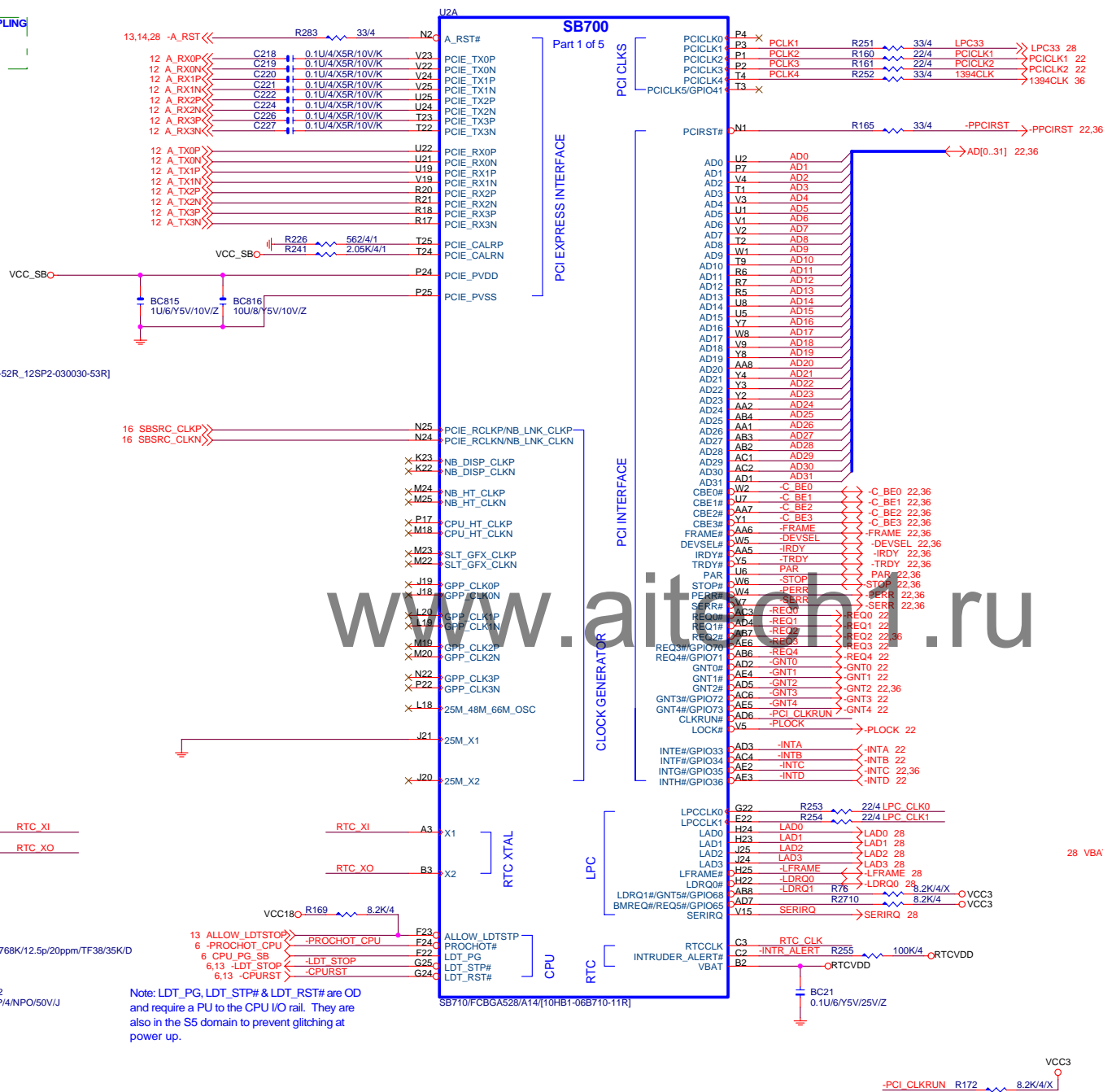
* the GFX_REFCLK input is required for all cases

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The diagram shows a square loop of wire with side length a . A vertical wire is positioned to the left of the loop, with a current I flowing upwards. A horizontal wire is positioned below the loop, with a current I flowing to the right. The vertical wire is at a distance x from the left side of the loop. The horizontal wire is at a distance $2a$ from the bottom side of the loop. The magnetic field B is indicated as pointing into the page.



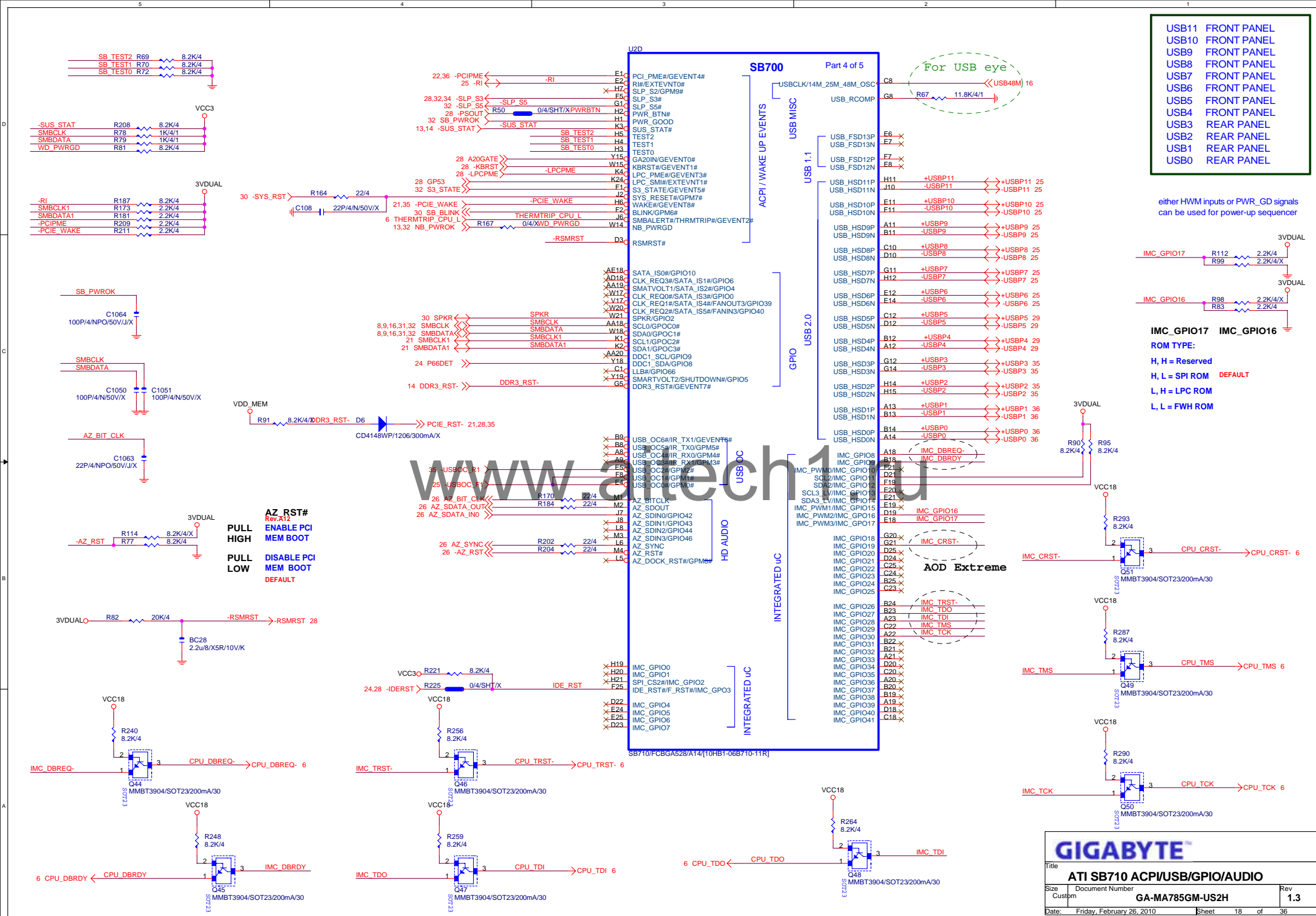
NOT ADD ICT FOR RTCVDD PIN

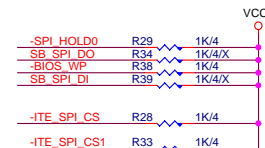
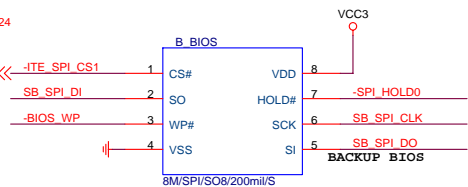
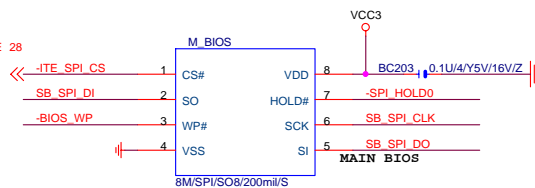
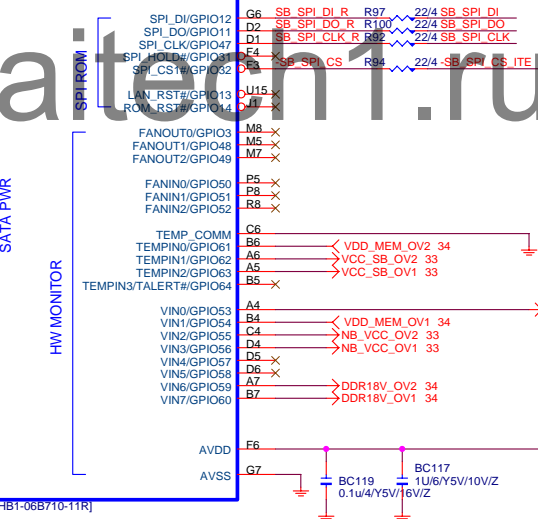
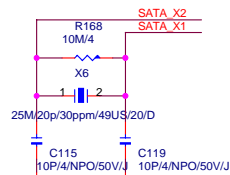
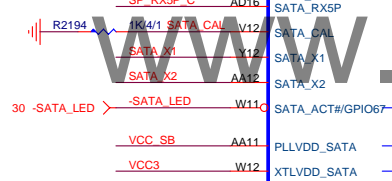
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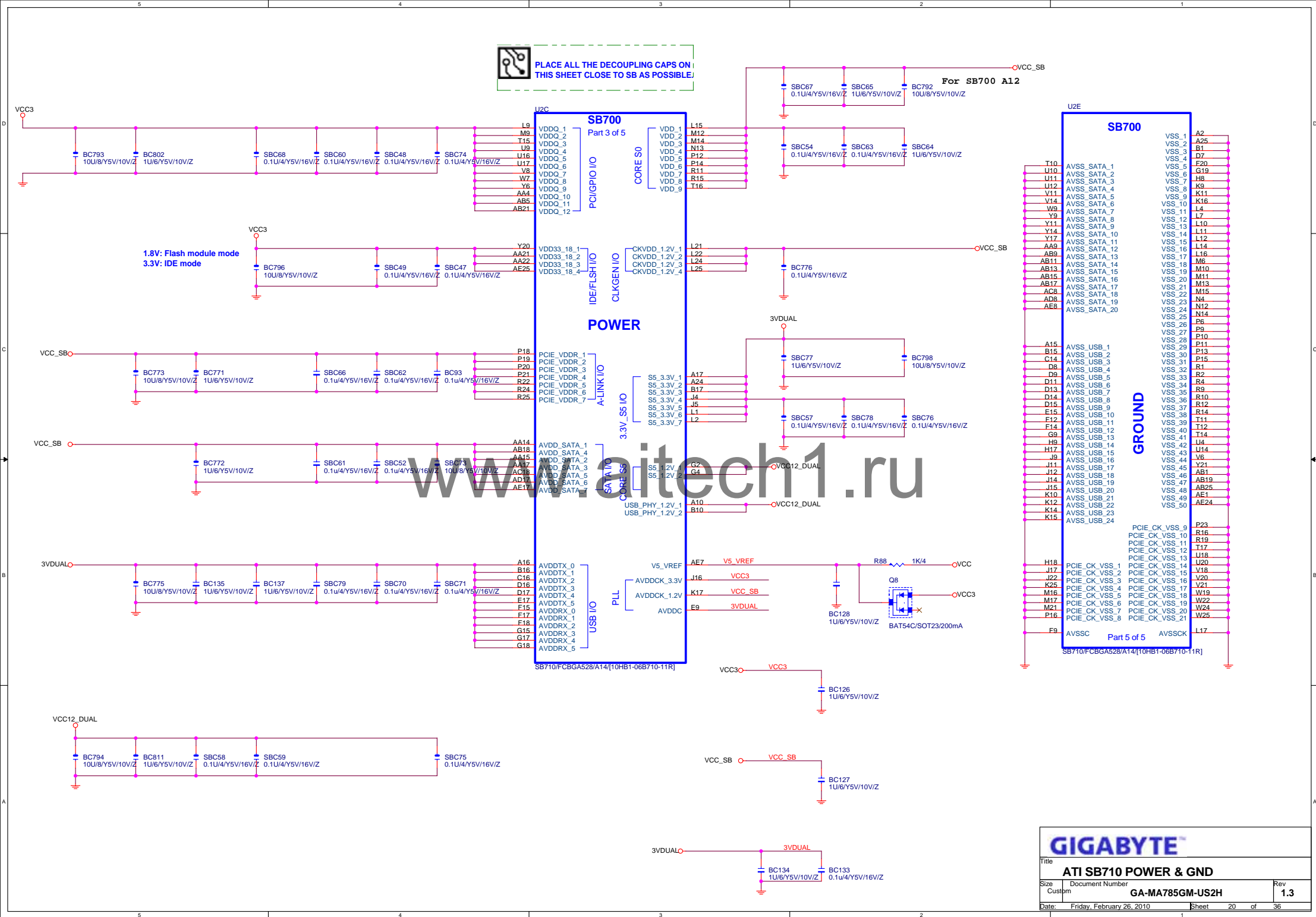
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ATI SB710 PCIE/PCI/CPU/LPC

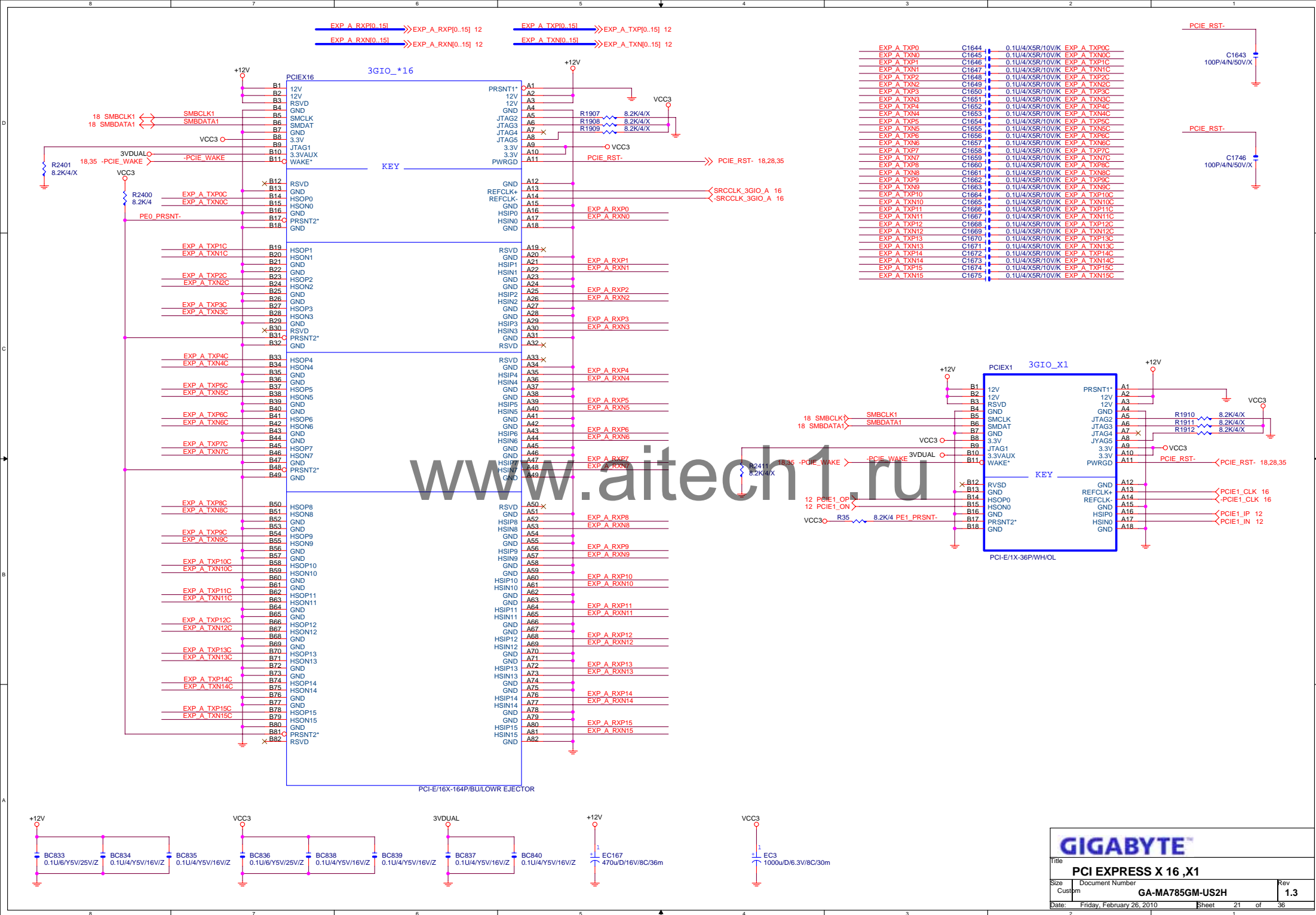
Size	Document Number
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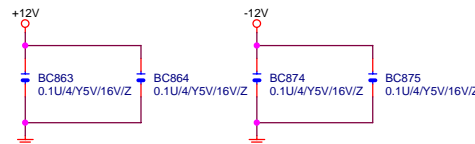
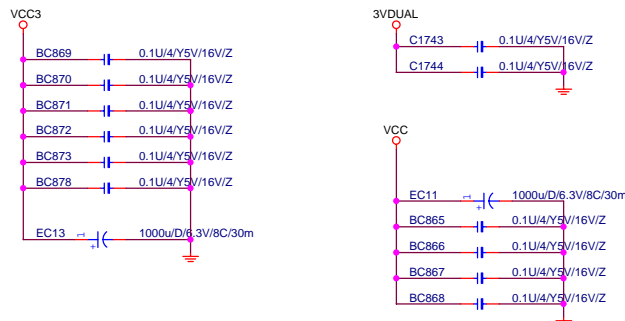
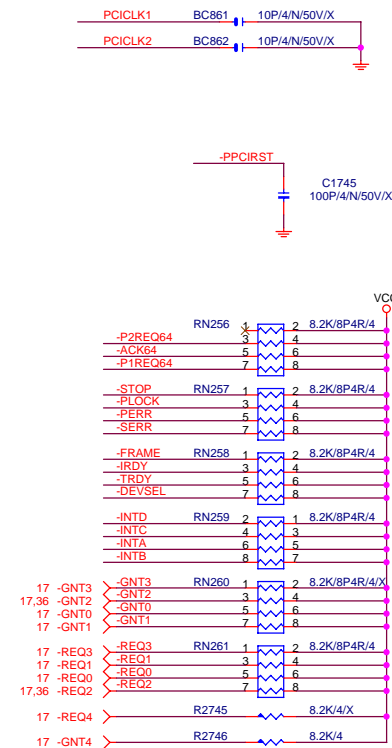
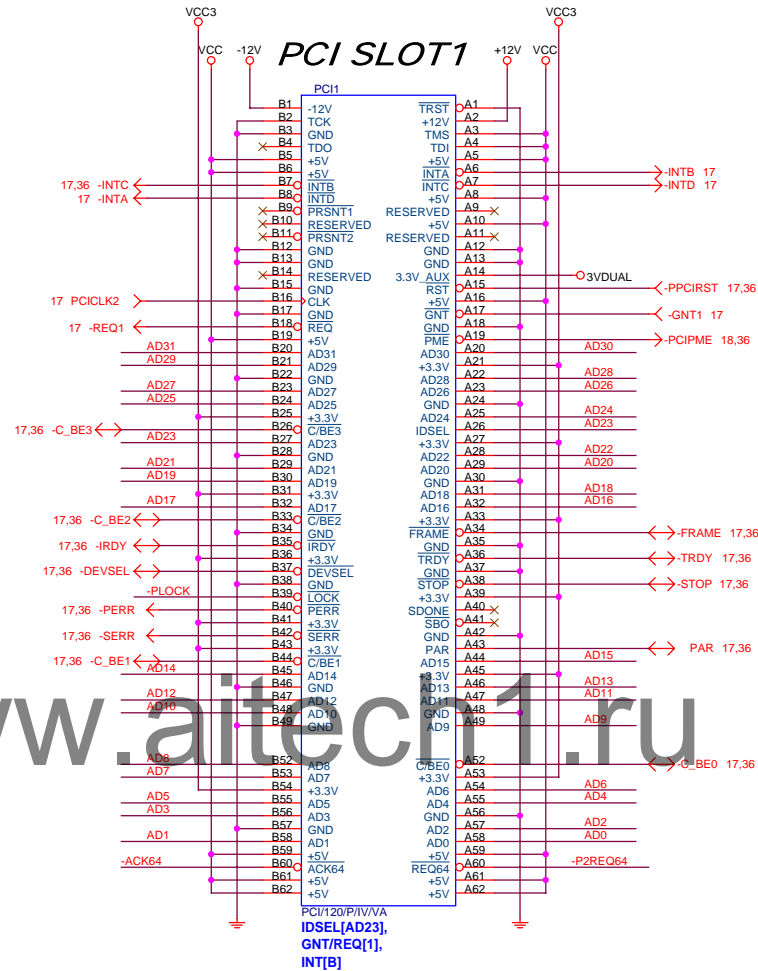
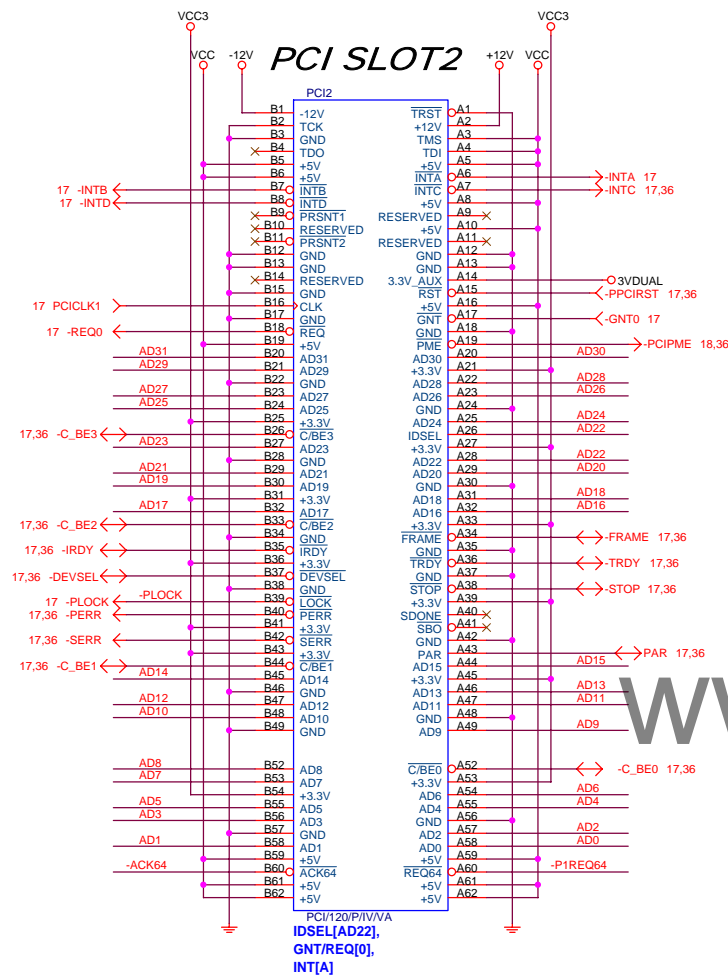






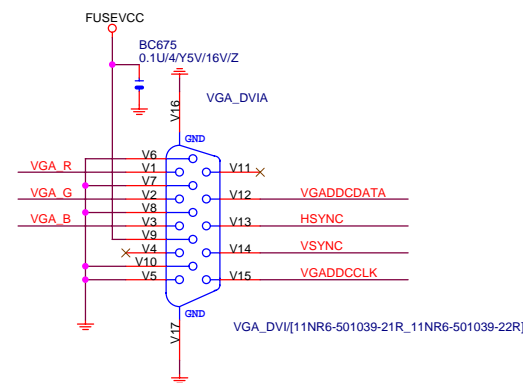
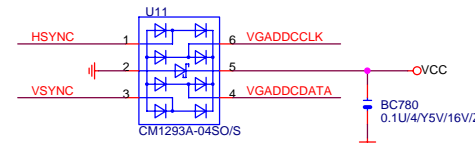
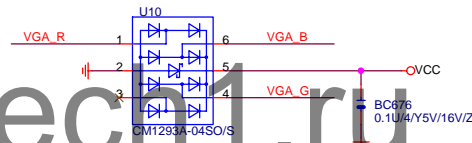
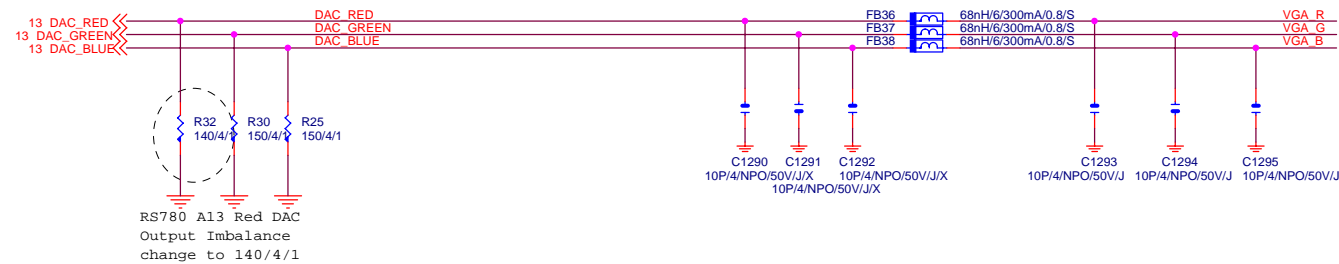
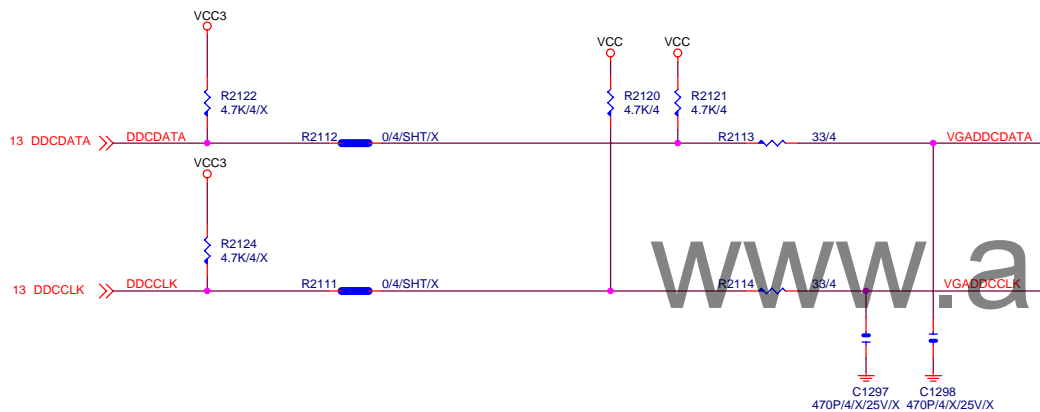
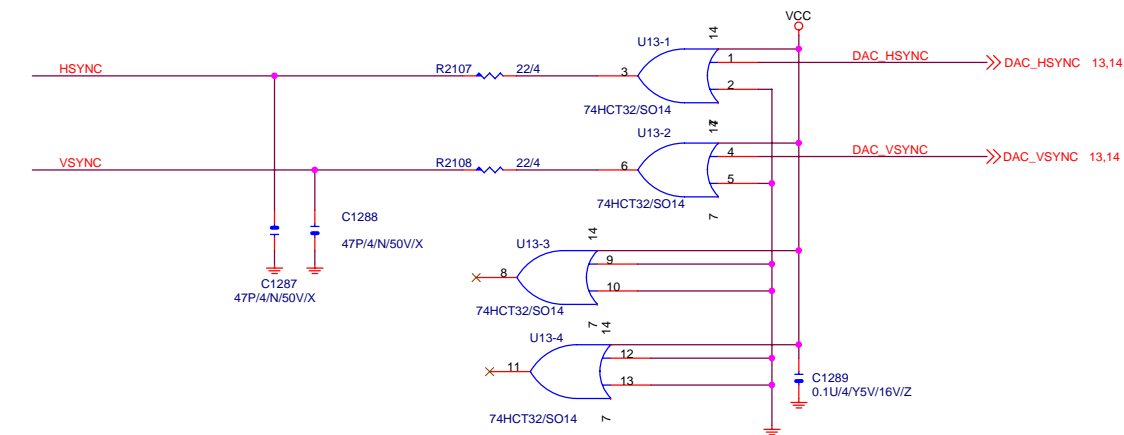
PCI SLOT 1,2

17,36 AD[0..31] ↔ AD[0..31]

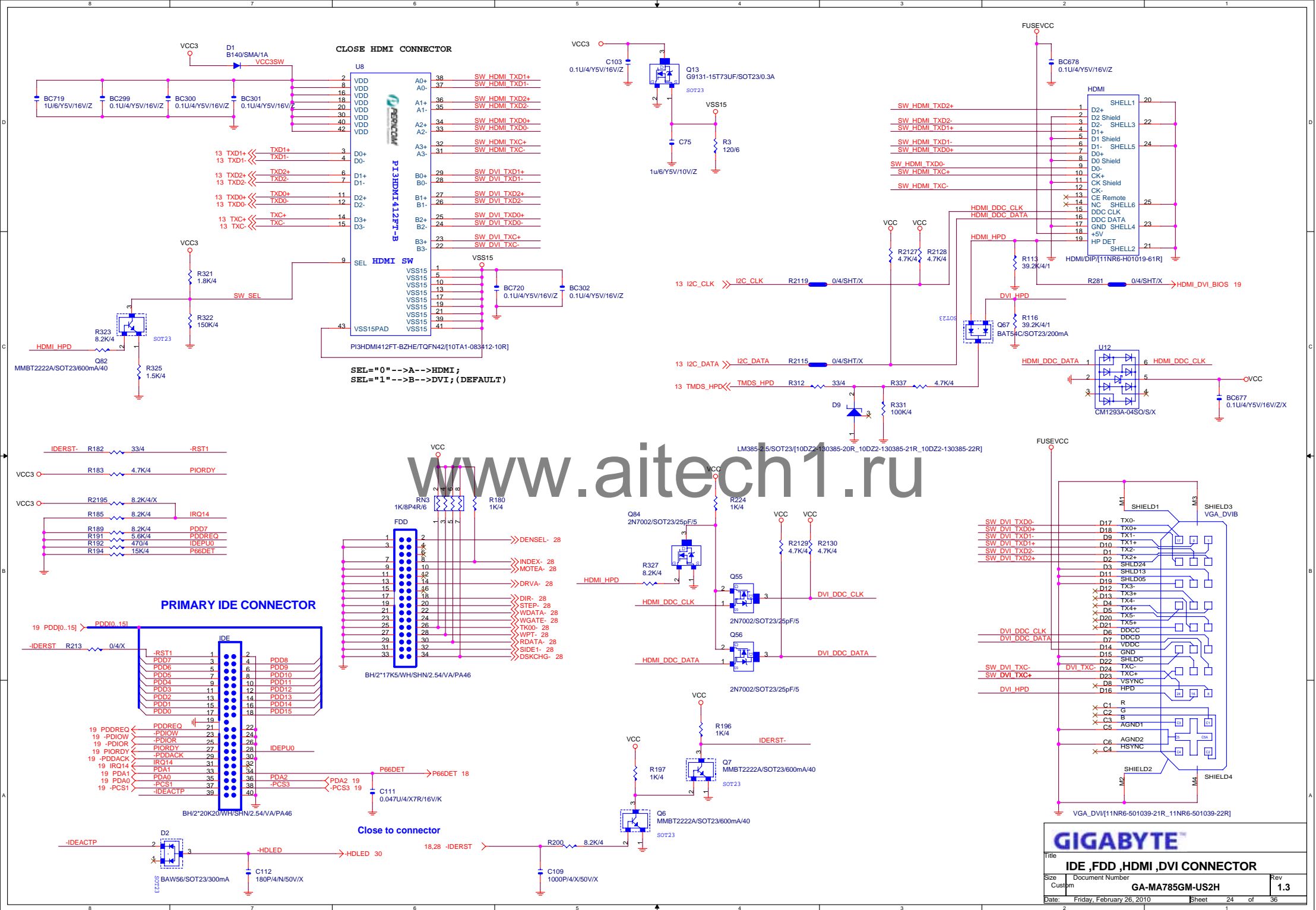


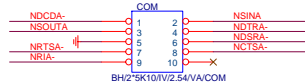
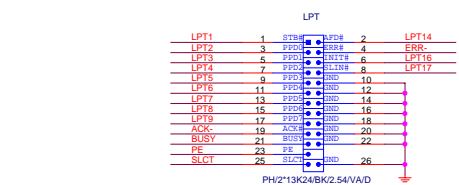
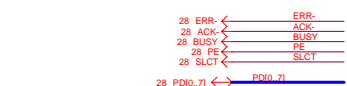
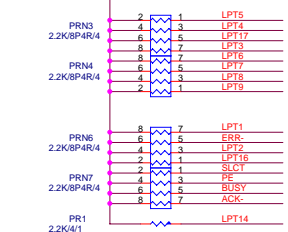
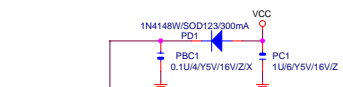
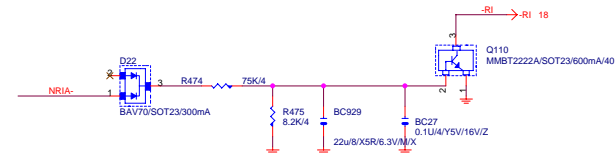
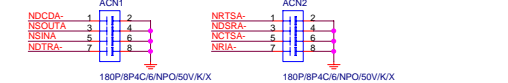
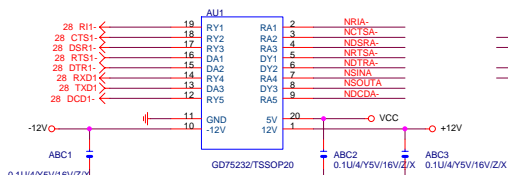
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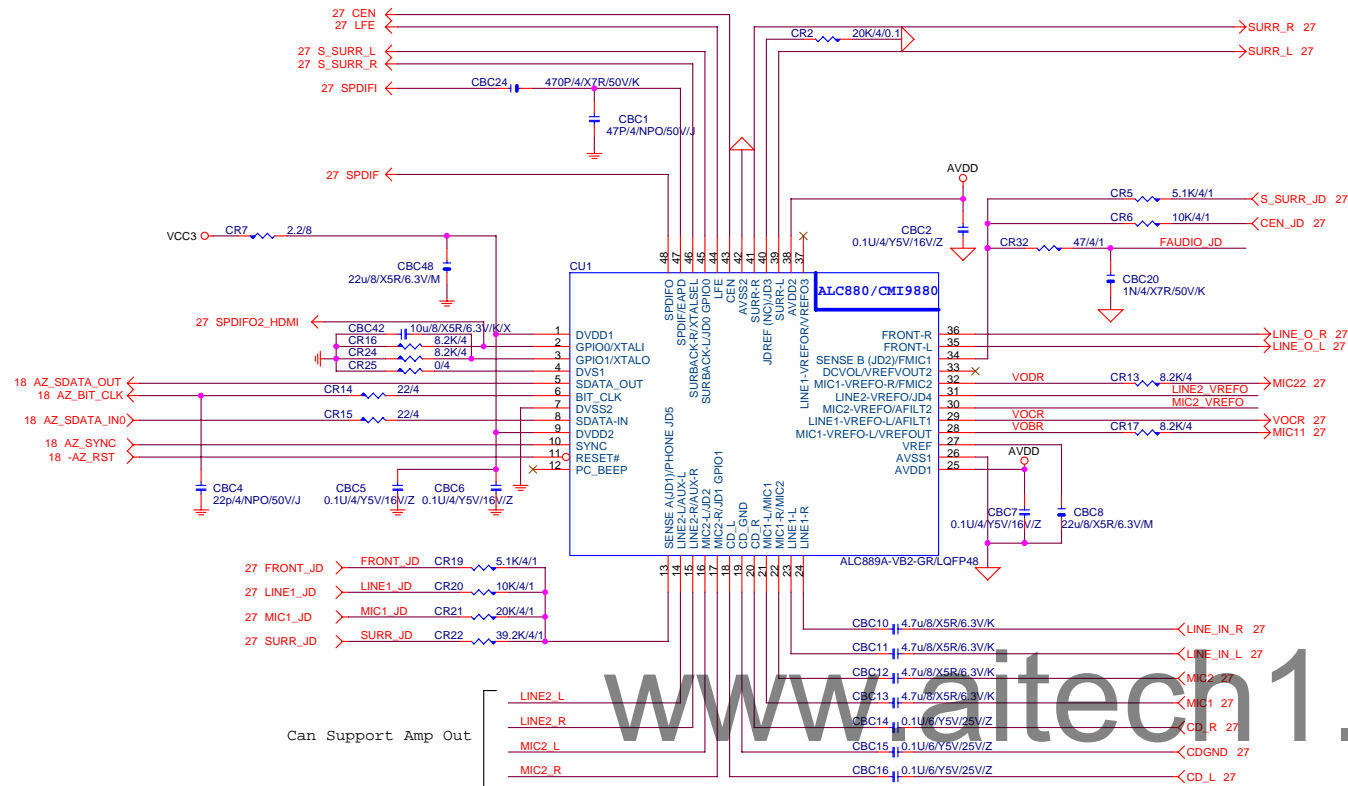
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Size Custom	Document Number GA-MA785GM-US2H	Rev 1.3
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RGB			
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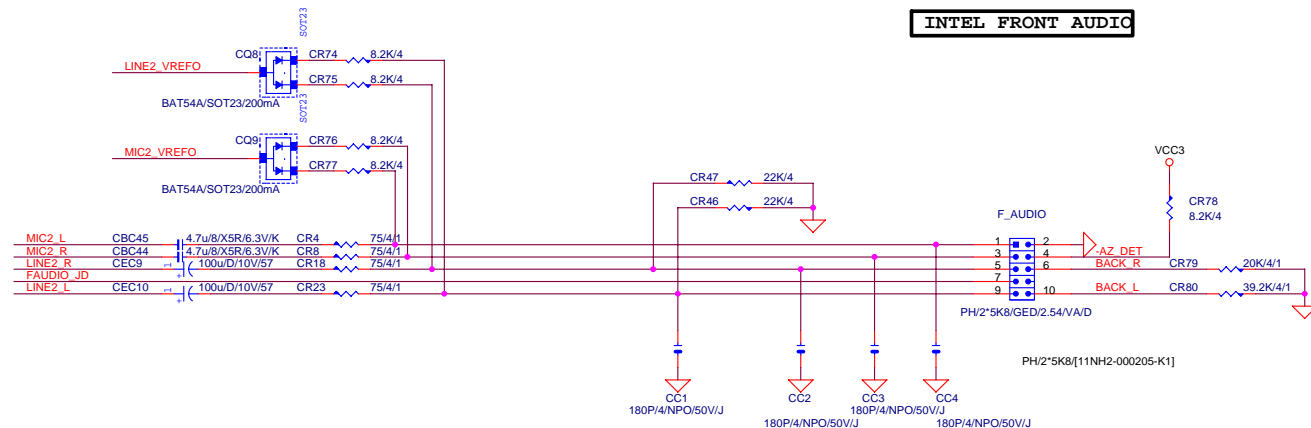






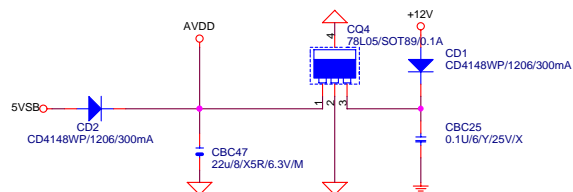
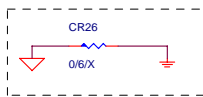
AZALIA CODEC ALC892/ALC889A/ Colay

	ALC892	ALC889A
CR16	X	O
CR24	X	O
CR25	X	O
CBC42	10uF/X5R	X
CR2	20K/1%	20K/0.1%
CR9	O	X
CR10	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR28/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	75 ohm

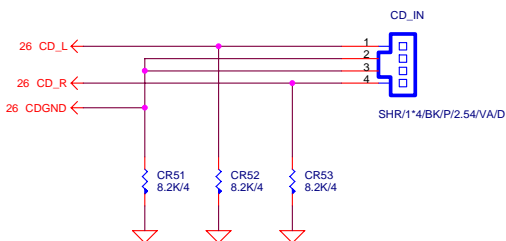


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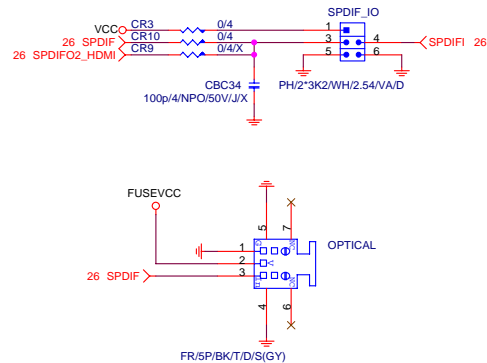
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Size	Document Number	Rev	
Custom	GA-MA785GM-US2H	1.3	
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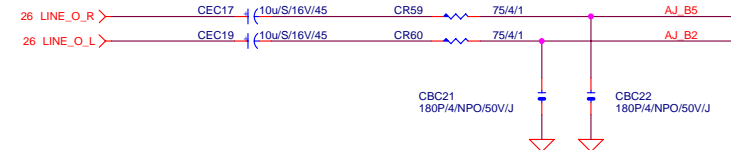
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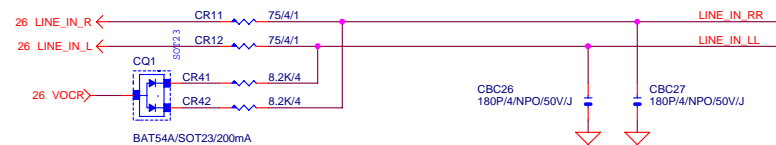
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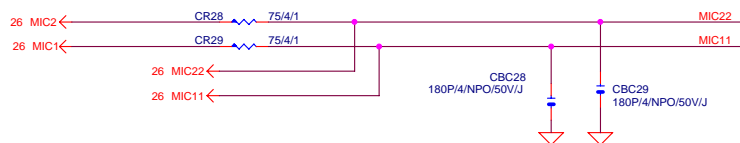
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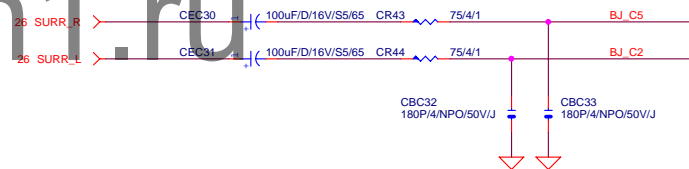
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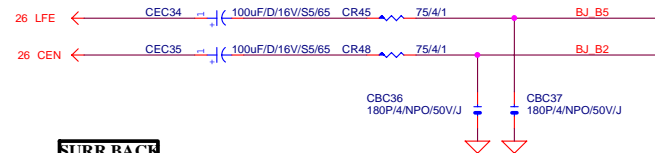
MIC



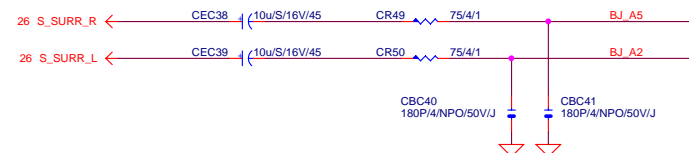
SURROUND



CEN/LFE

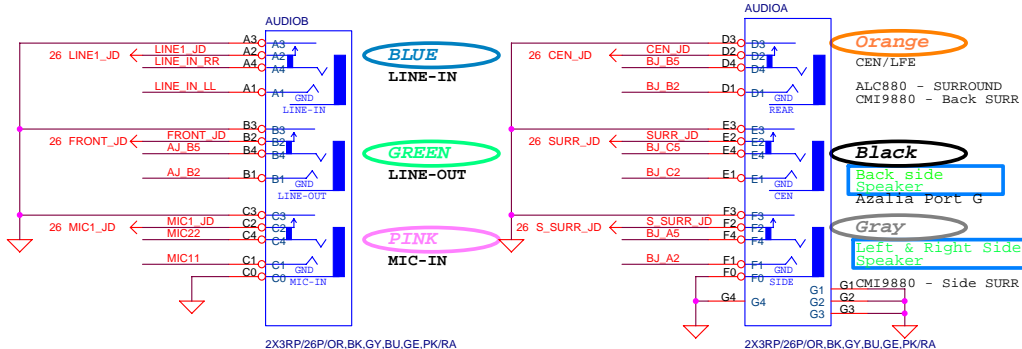
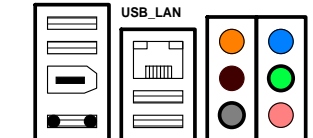


SURR BACK



For Audio precision test
CR27 0.01uF/6.3V/50V/K

USB_1394_ESATA

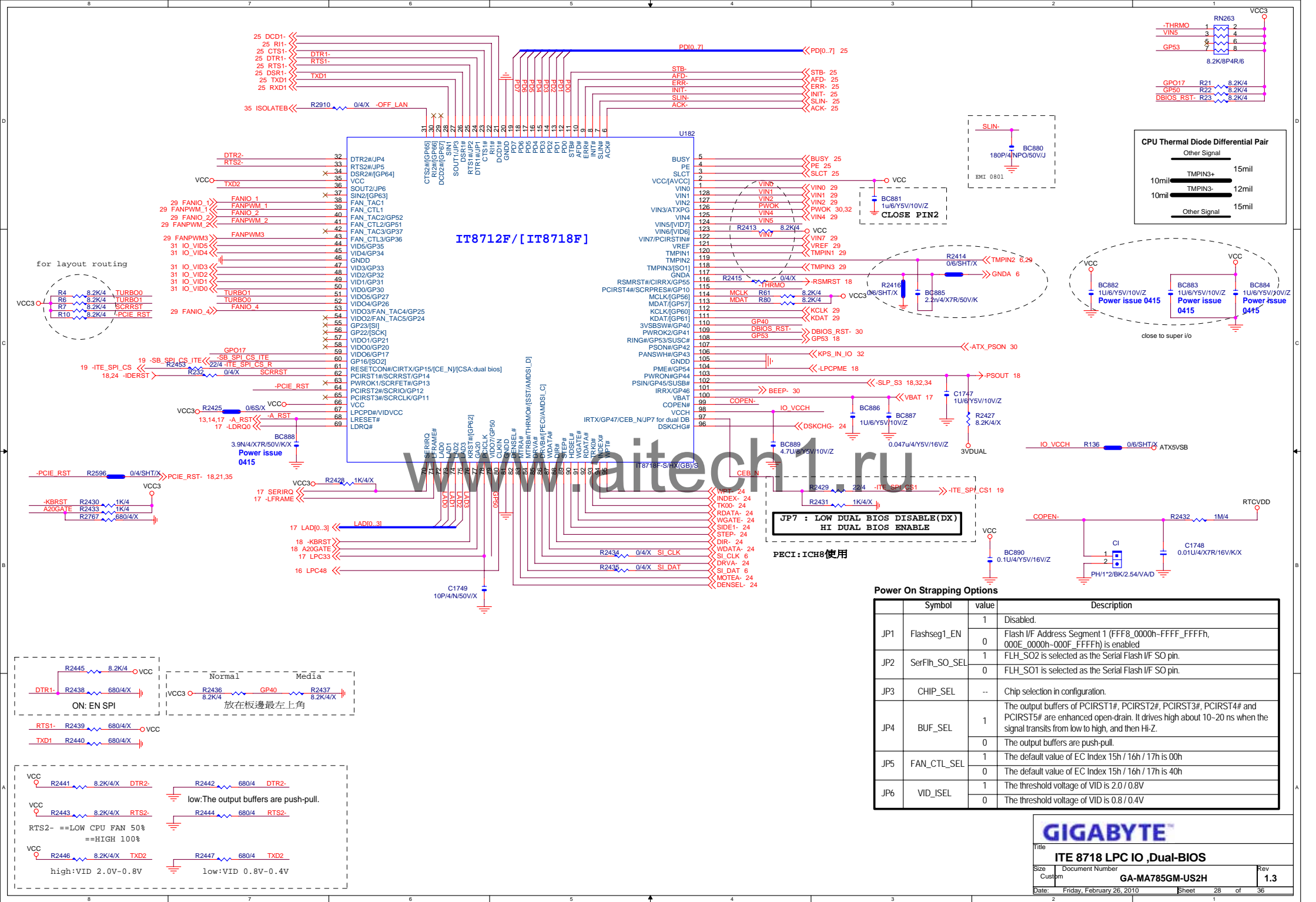


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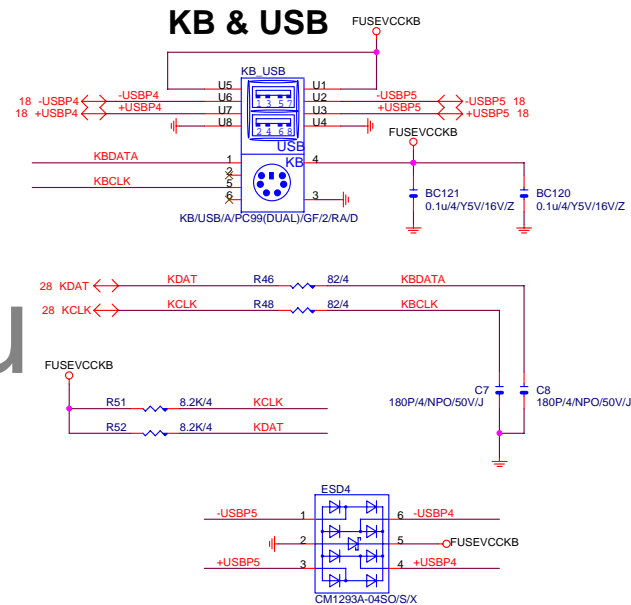
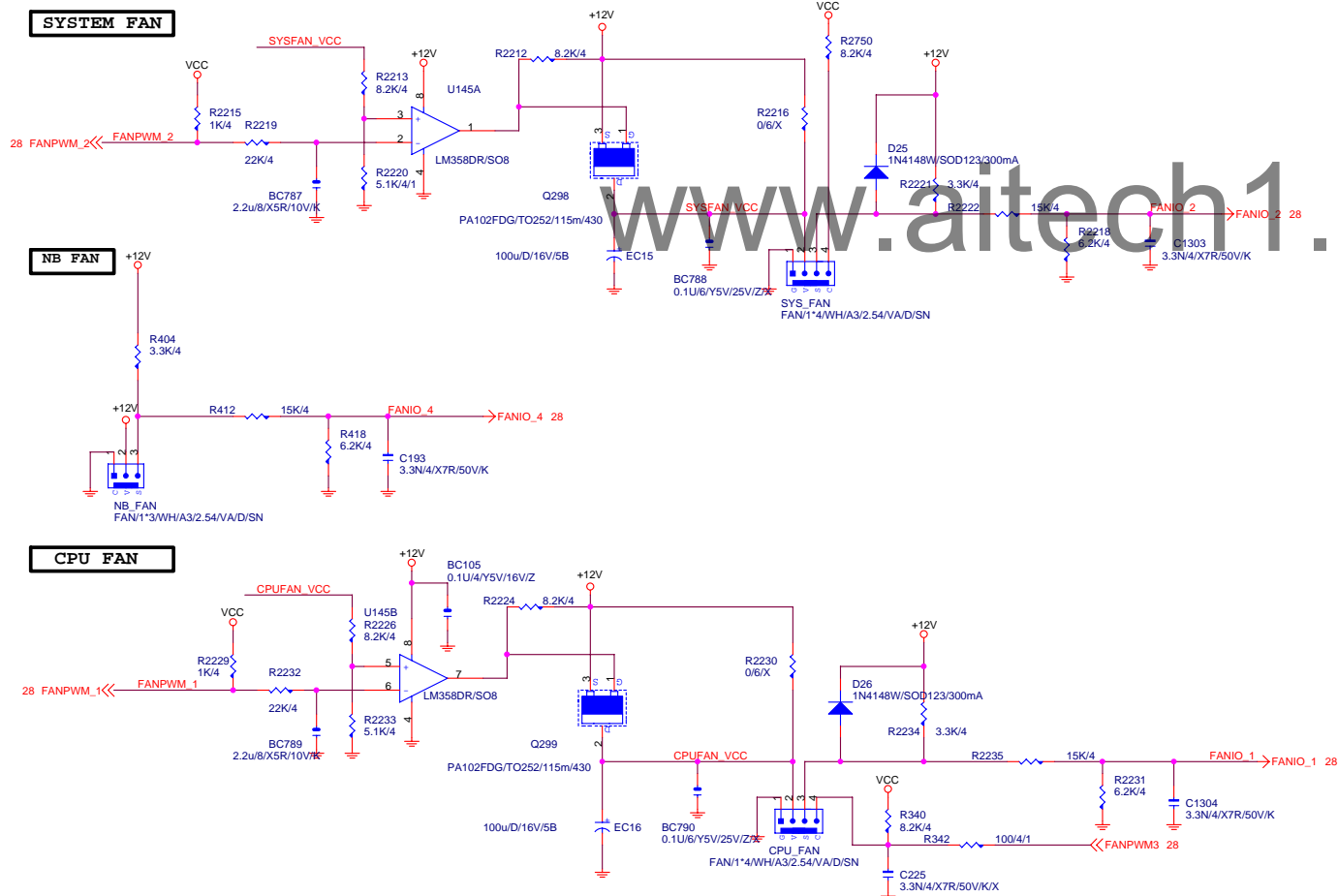
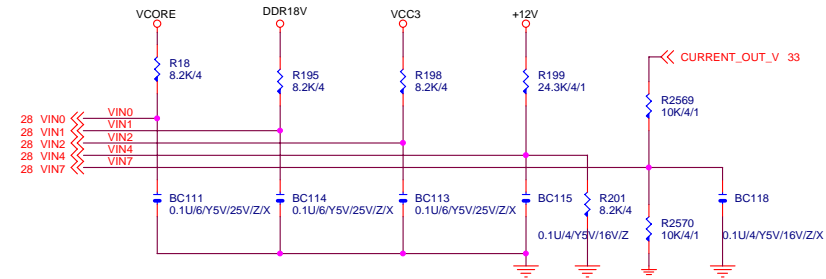
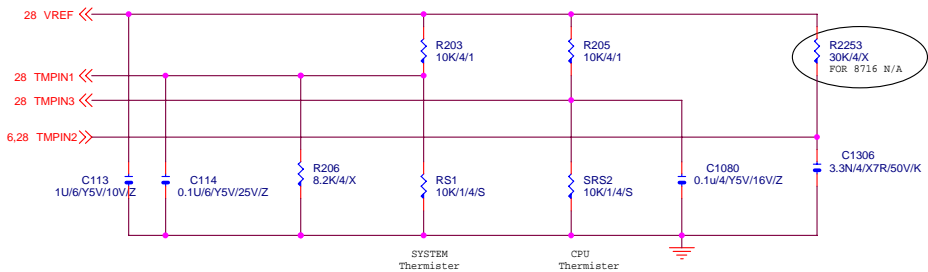
A3R7/13P/0BG/[11NR6-403006-71]
3RJ+15P/[11NR6-403004-31]

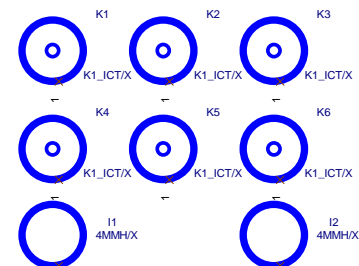
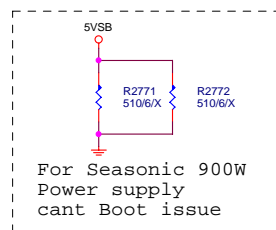
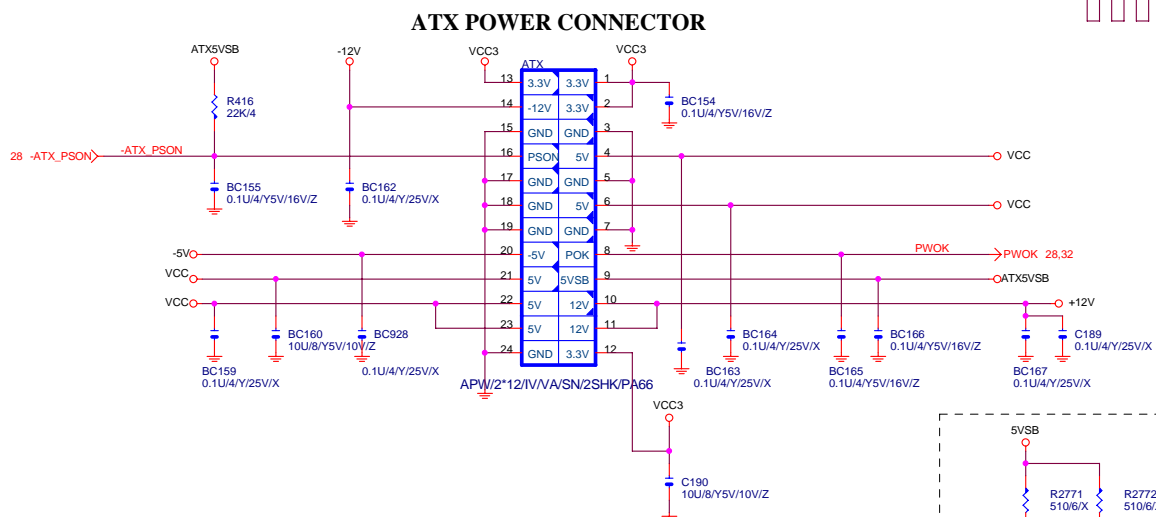
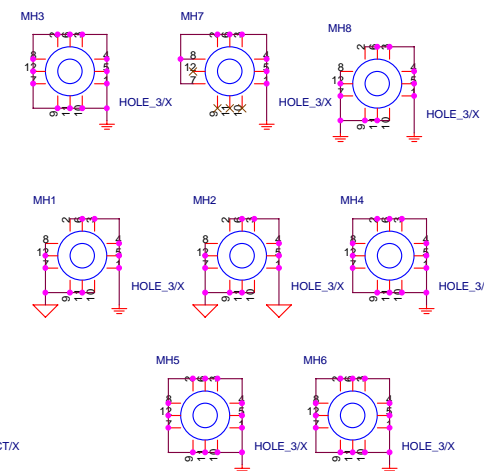
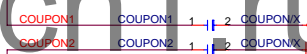
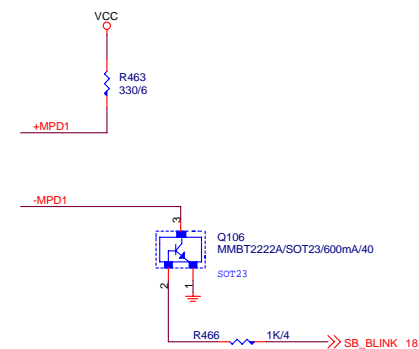
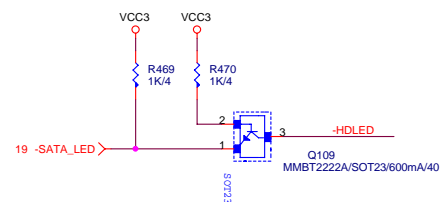
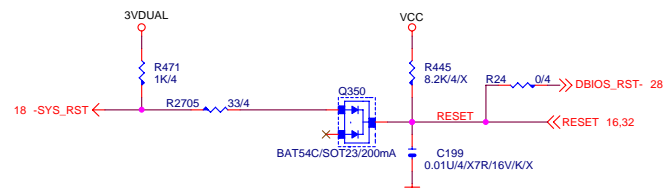
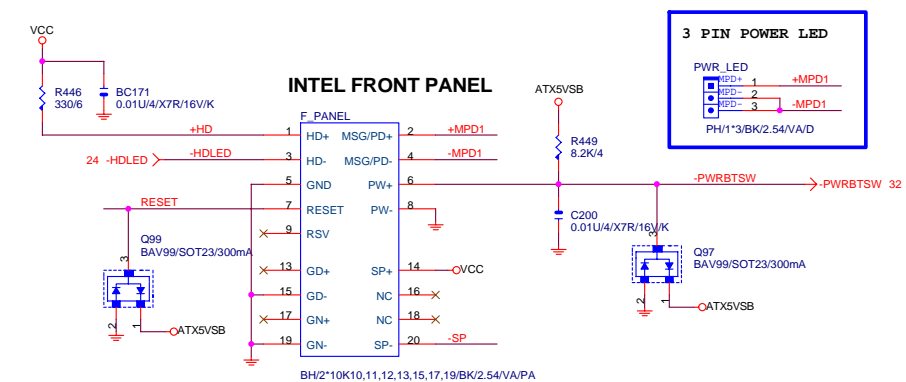
GIGABYTE

Title		
AUDIO JACK		
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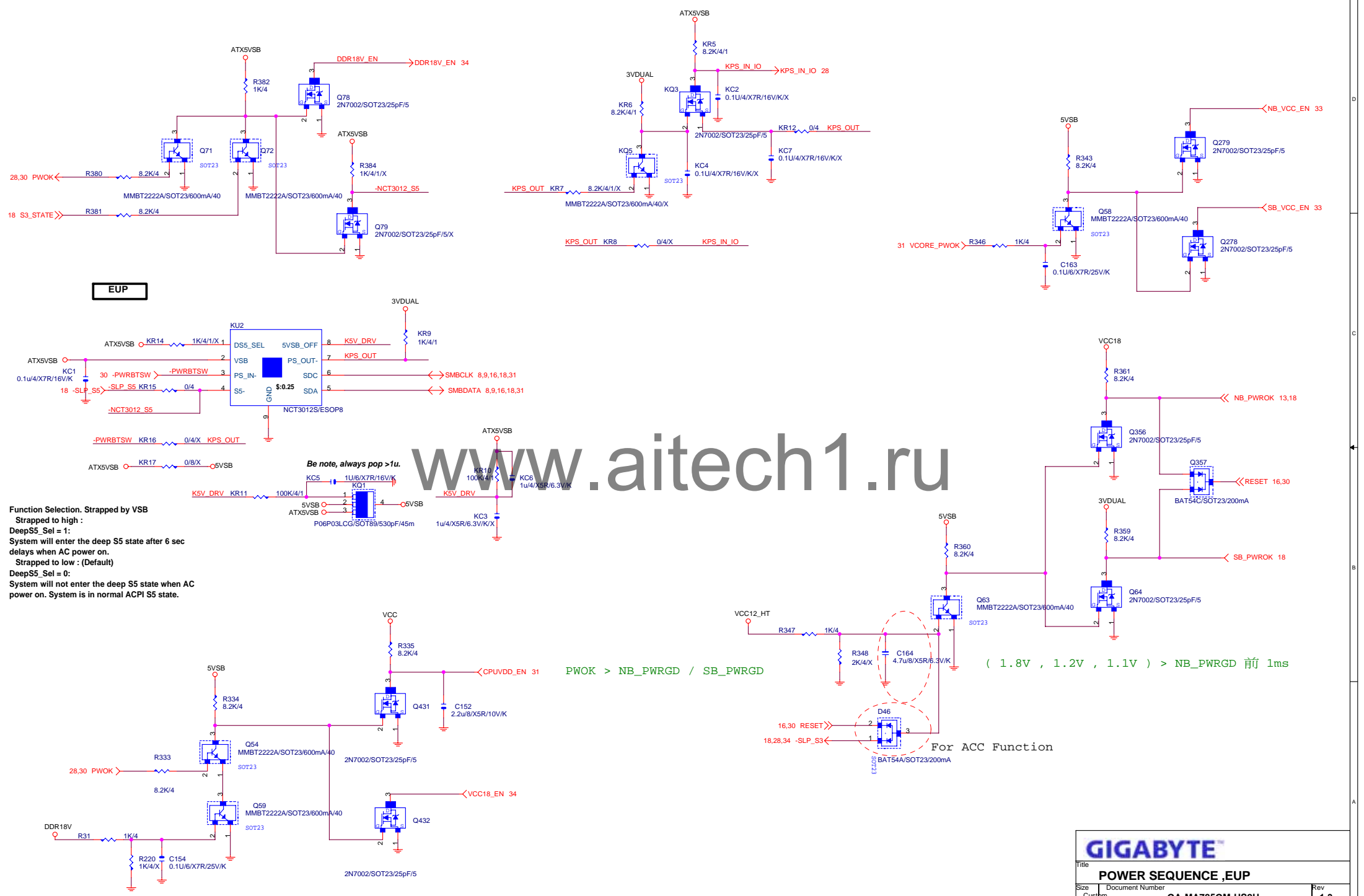


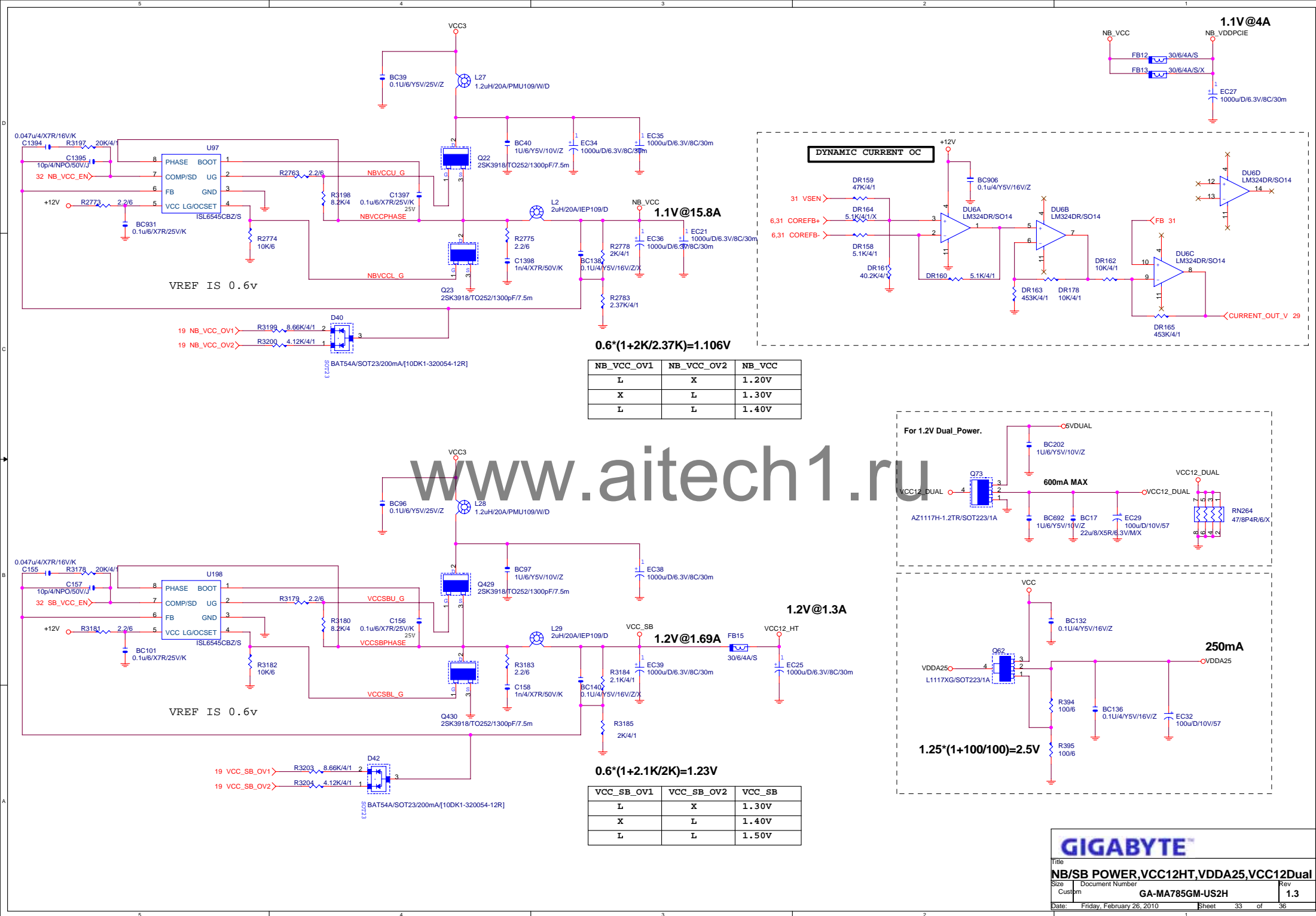
Hardware Monitor circuits





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VCORE (PWM ISL6324A+6612A)			
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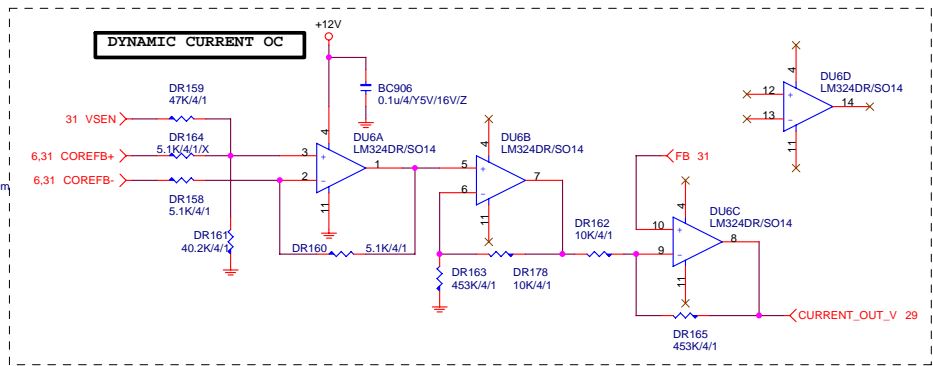




VREF IS 0.6v

$0.6 \times (1 + 2K/2.37K) = 1.106V$

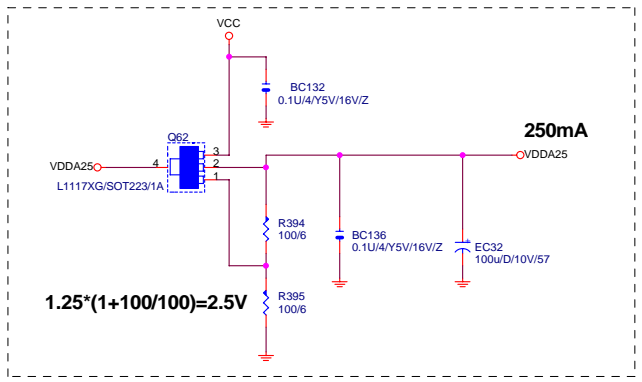
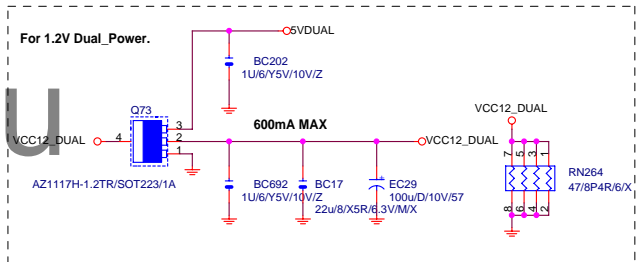
NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V

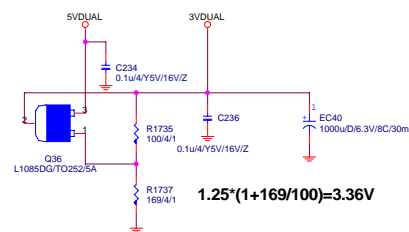
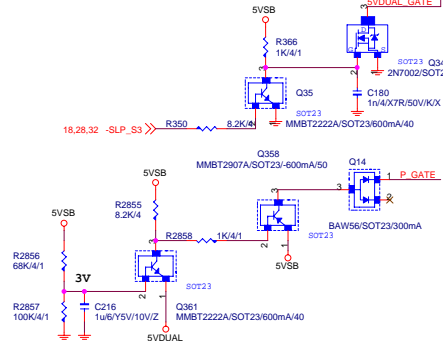
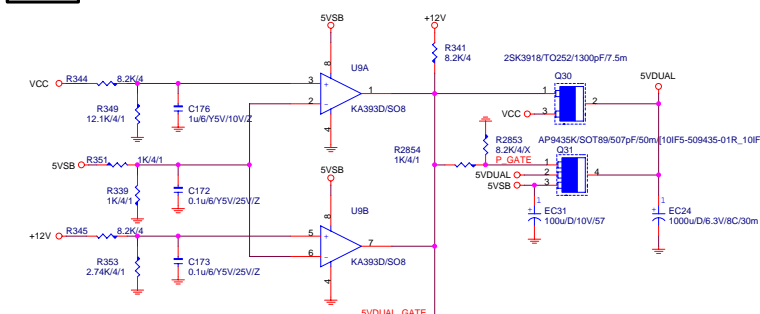


VREF IS 0.6v

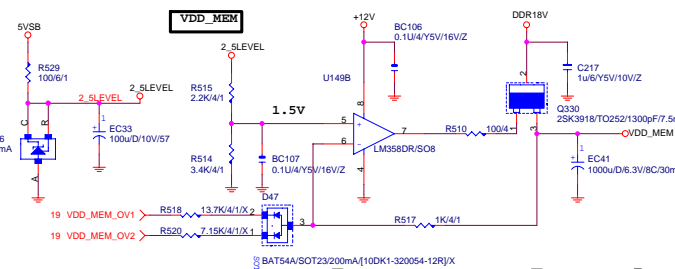
$0.6 \times (1 + 2.1K/2K) = 1.23V$

VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

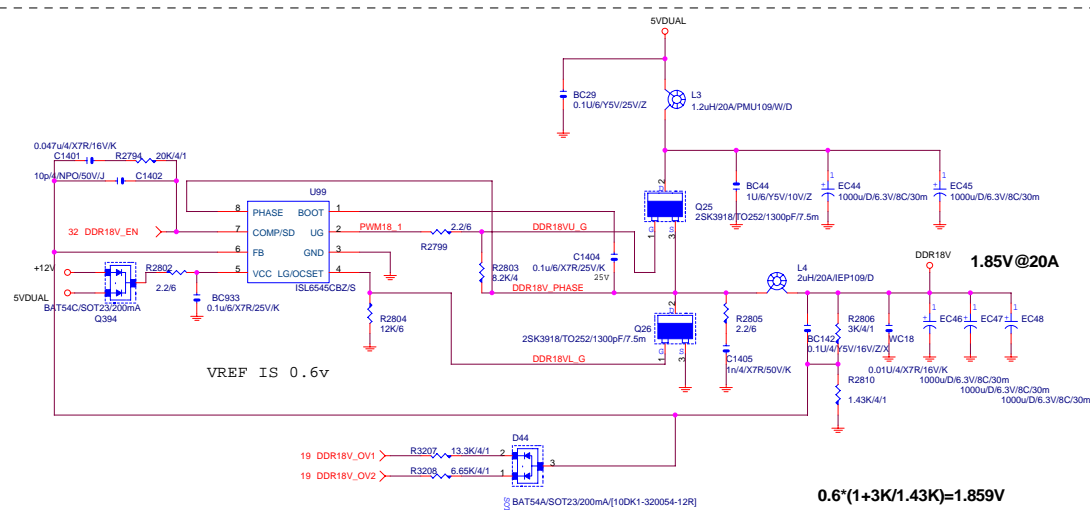
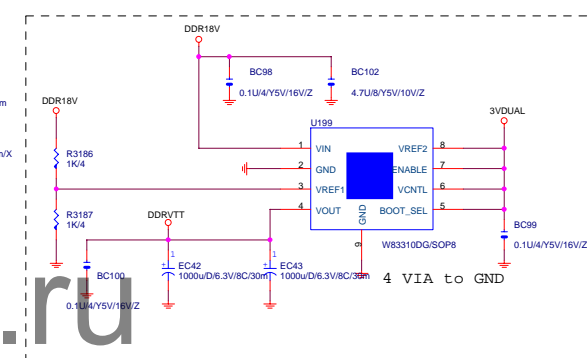




$$1.25 \times (1 + 169/100) = 3.36V$$

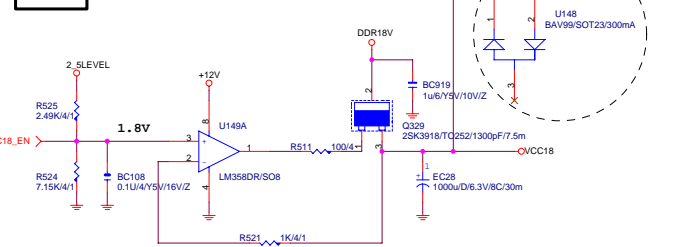


VDD_MEM_OV1	VDD_MEM_OV2	VDD_MEM
L	X	1.60V
X	L	1.70V
L	L	1.80V



$$0.6 \cdot (1 + 3K/1.43K) = 1.859V$$

DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V



ATI for vcc3/vcc18 power ramp-up 2.1V



Title			
DDRII POWER , VCC18			
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PCIE-1G LAN

LR33:0/6 DISABLE SWITCHING REG

LR16:
RTL8101E-->2K/4/1
RTL8111C/8102E-->2.49K/4/1

RTL8111C

LR36:
RTL8101E/8102E -->X
RTL8111C-->O

LU1

RTL8111C-VCO-GR/EN64

18,21 -PCIE_WAKE -PCIE_WAKE
18,21,28 PCIE_RST- PCIE_RST-

12 ML_OP ML_OP
12 ML_ON ML_ON
16 SRCCLK_LAN SRCCLK_LAN
16 -SRCCLK_LAN -SRCCLK_LAN

12 ML_IP ML_IP
12 ML_IN ML_IN

CLOSE LAN CHIP

USB_LAN CONNECTOR

RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8102E:LC5/LC6-->O
RTL8111C:LC6-->O

RTL8102E -->X

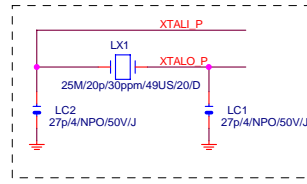
CLOSE LAN CHIP

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

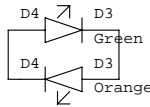
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1

USB_LAN

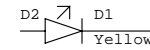
USB+LAN/1G/GO,Y/OS/RA/D/1C



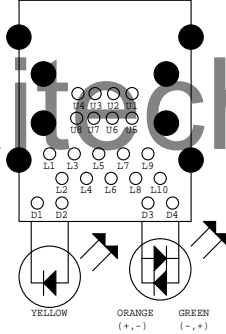
Dual Color LED



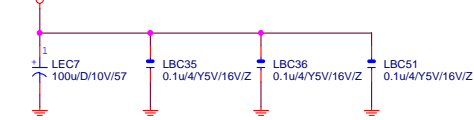
Single Color LED



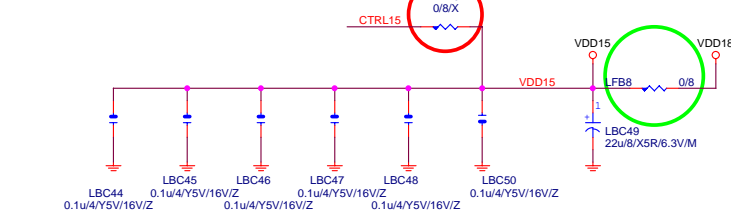
P35-152-19W9



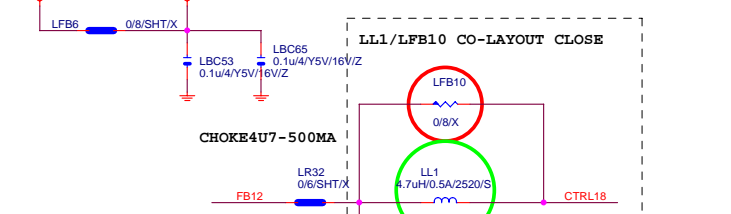
3VDUAL



CTRL15



3VDUAL



LL1/LBC64/LBC63

CLOSE LU1 PIN1

FOR 93C46 OR BIOS DETECT

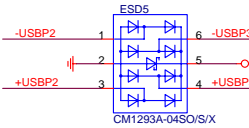
RTL8102E -->X

USB_LAN

EMI



18 -USBP2 -USBP2
18 +USBP2 +USBP2
18 -USBP3 -USBP3
18 +USBP3 +USBP3



GIGABYTE

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